CHAPTER 4

PULSE WIDTH MODULATION SCHEMES IN THREE-LEVEL VOLTAGE SOURCE INVERTERS

4.1 Introduction

Semiconductor switch ratings have limited the application of power converters rated in the tens to hundreds of megawatts. Large inverters operating at these power levels in the medium voltage range (2-13 kV) have traditionally been the domains of gate turn off (GTO) thyristors. However, their switching speed is severely limited compared to the IGBT's so that the carrier frequency of a GTO inverter is generally only a few hundred hertz. High switching frequencies can be achieved by replacing each of the slower switches so that each individual IGBT shares the dc link voltage with others in the string during its off state. The devices are operated in saturation region of operation. This is because there exists higher losses in active region operation of these devices.

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The applications involved in synthesis of a quality power, medium to high voltage range include motor drives, power distribution, power quality, and power conditioning applications.

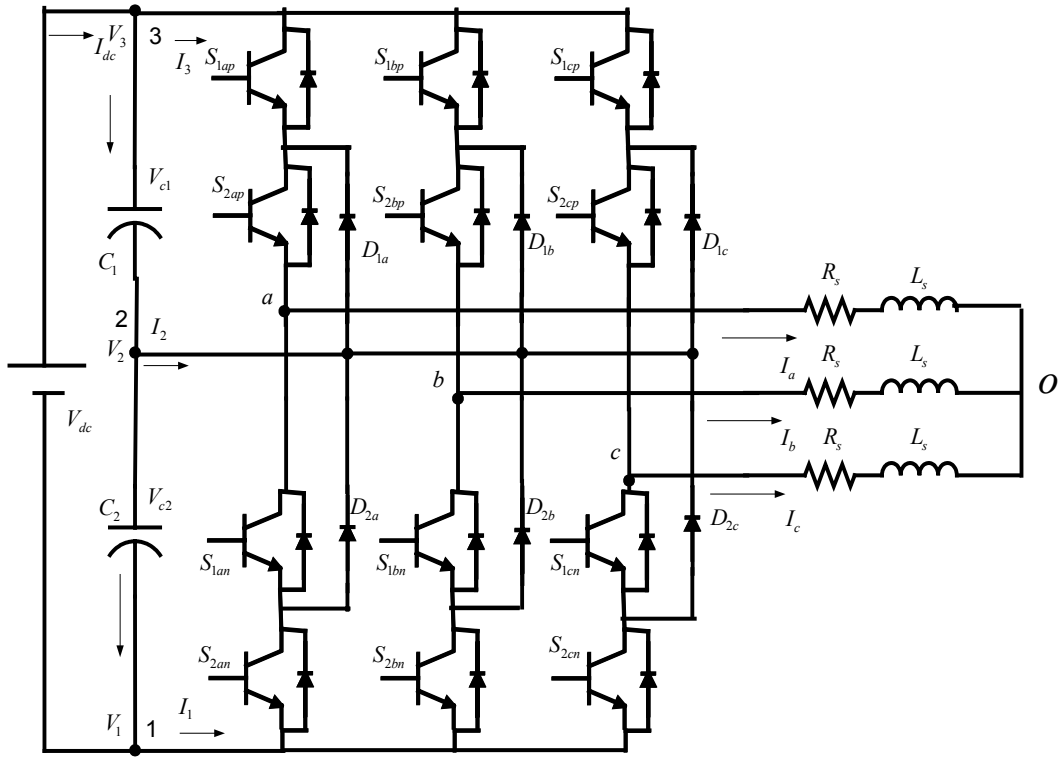
Desirable Characteristics of Three Phase Three Level PWM VSI

- Wide linearity of operation.
- Minimum switching losses.

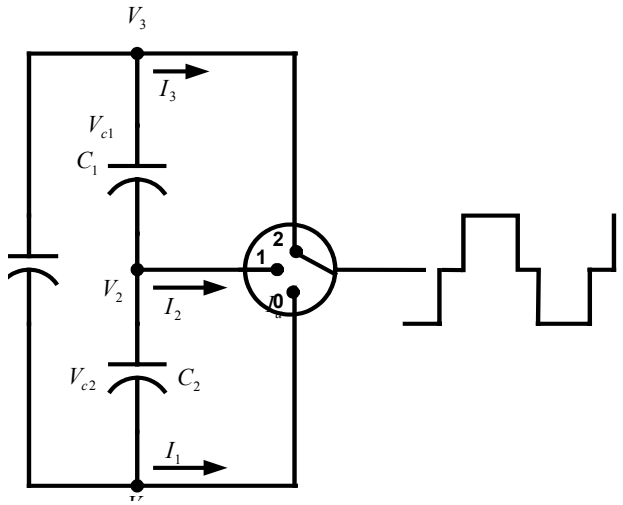
- Minimum voltage and current harmonics.
- Controlled neutral point voltage and current to ensure stiff capacitor voltages.
- To obtain steps in the output voltage.

4.2 Model of Three-Level Diode Clamped Inverter

A three-level diode clamped inverter is shown in Figure 4.1. In this circuit, the dc bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors "2" can be defined as the neutral point. The output voltage has three states: $V_{dc}/2$, 0, $-V_{dc}/2$. The devices are switched in combinations to obtain these levels in the voltage waveform. The switching combination of the top two devices is termed as H_{i3} (S_{1ip}, S_{2ip}), the middle two devices as H_{i2} (S_{2ip}, S_{1in}), and the bottom two devices as H_{i1} (S_{1in}, S_{2in}) (i=a, b, c). When the two top devices are switched on the converter switches to the $+V_{dc}/2$, when the middle two devices are turned on, the converter switches to the zero voltage, and when the bottom two devices are switched on, the converter switches to $-V_{dc}/2$. The pole representation and output waveform of the three-level inverter is shown in Figure 4.1 (II). The turn-on and turn-off sequences of any of the switching devices of the inverter are represented by existence functions ($H_{i3,}$ H_{i2}, H_{i1}), which have a value of unity when it is turned on and becomes zero when it is turned off. The three-phase voltage equations for star-connected, balanced three-phase loads are expressed in terms of the existence functions and input DC voltages. The operation of the converter is explained in section 3.1.



(I)



(II)

Figure 4.1: (I) Schematic of Three-Level Voltage Source Inverter (II) Representation of three-level inverter using the concept of poles.

The output phase voltage of the inverter is given by

$$v_{ao} = H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10} \tag{4.1}$$

$$v_{bo} = H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10} \tag{4.2}$$

$$v_{co} = H_{c3}V_{30} + H_{c2}V_{20} + H_{c1}V_{10}\,. \tag{4.3}$$

The switches are assumed ideal as is common in preliminary functional analysis of switching power converters. These assumptions include: (a) negligible forward voltage drop of the switch throws in their on-state; (b) sufficient on-state current carrying capacity and of-state voltage blocking capacity commensurate and compatible with the voltage and current ratings of the system; and (c) negligible transition periods between turn on and turn off of the switch throws that permit repetitive high frequency switching. The voltages at the throw terminals of the switch are assumed stiff such that their variations during a switching period can be neglected. Similarly, the switch currents are assumed stiff such that their variations over a switching period can be neglected. These assumptions essentially allow the focus to be on the power transfer process and the functional features. In practical power converters, filter elements appropriately applied at the input and output ports of the system would ensure that these assumptions are valid. In order to maintain continuity of the three phase currents connected to the poles, at least one of the throws connected to any given pole of the switch has to be closed. Furthermore, each current port may be connected to only one voltage terminal at any given instant of time. Otherwise, two stiff voltages will be short-circuited together, resulting in uncontrolled currents through the switch throws. As a result, no more than one combination of switches is on at any given instant of time. Hence the following conditions are to be followed when switching the devices of a multilevel converter.

$$H_{a3} + H_{a2} + H_{a1} = 1 \tag{4.4}$$

$$H_{b3} + H_{b2} + H_{b1} = 1 \tag{4.5}$$

$$H_{c3} + H_{c2} + H_{c1} = 1 \tag{4.6}$$

From Eq. (4.4),

$$H_{a2} = 1 - H_{a1} - H_{a3}. \tag{4.7}$$

Substituting the condition in Eq. (4.7) in (4.1), gives

$$v_{ao} = H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20}. \tag{4.8}$$

Similarly for the other phases,

$$v_{bo} = H_{b3}V_{c1} - H_{b1}V_{c2} + V_{20} \tag{4.9}$$

$$v_{co} = H_{c3}V_{c1} - H_{c1}V_{c2} + V_{20} \tag{4.10}$$

where V_{20} is the voltage between the neutral of the supply and the common point of the two capacitors. This is known as the neutral voltage, which is floating, and can assume any voltage and becomes the control variable and used for controlling the neutral point voltage.

The node currents of the inverter are given by Eqs. (4.11 - 4.13). Consider the node 3; the node current is available when the top devices of each leg are switched on, which provides the path for the current; i.e., when the top two devices in phase "a" are turned on, current I_a passes through these devices and similarly for the other phases b and c.

$$I_3 = H_{a3}i_a + H_{b3}i_b + H_{c3}i_c \tag{4.11}$$

$$I_2 = H_{a2}i_a + H_{b2}i_b + H_{c2}i_c \tag{4.12}$$

$$I_1 = H_{a1}i_a + H_{b1}i_b + H_{c1}i_c. \tag{4.13}$$

Writing the Kirchoff's Current Law (KCL) equation at node 3 gives the differential equation of the capacitor voltage V_{c1} and KCL equation at node 1 gives differential equation for capacitor voltage V_{c2}.

$$C_1 pV_{c1} = -I_{dc} + H_{a3} i_a + H_{b3} i_b + H_{c3} i_c . \tag{4.14}$$

$$C_2 pV_{c2} = -\left(I_{dc} + H_{a1} i_a + H_{b1} i_b + H_{c1} i_c\right). \tag{4.15}$$

Multilevel converters can be modulated using the following two methods:

- Direct digital technique SVPWM.
- Carrier-based (triangular comparison) technique.

The direct digital technique involves utilization of space vector approach wherein the duty cycles for the switching inverter are calculated. The gating signals are presequenced and stored as lookup table for the available switching states of a multilevel inverter. Carrier-based PWM utilizes the per cycle volt-second balance to synthesize the desired output voltage waveform.

Consider the carrier-based sine-triangle pulse width modulation; the different types of the carrier-based techniques are available and mentioned in the literature review. In the previous carrier-based PWM schemes, it uses (N-1) triangular carrier waveforms and single modulation signal to obtain the switching pulses. Different carrier-based techniques are explained in Chapter 3.

4.3 Carrier-Based Sine-Triangle Pulse Width Modulation

In the proposed carrier-based PWM scheme, the switching function for each device is determined such that the devices are switched independently. In the PWM

scheme, single carrier waveform and N modulation signals are used. The concept of sharing functions is introduced in this section.

4.3.1 Three-Level Inverter

The output voltages of the three level inverter is defined by the following equations

$$v_{ao} = H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10} \tag{4.16}$$

$$v_{bo} = H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10} \tag{4.17}$$

$$v_{co} = H_{c3}V_{30} + H_{c2}V_{20} + H_{c1}V_{10}. \tag{4.18}$$

The switching constraints to be followed in order to avoid the shorting of the dc bus voltage source are

$$H_{a3} + H_{a2} + H_{a1} = 1 \tag{4.19}$$

$$H_{b3} + H_{b2} + H_{b1} = 1 \tag{4.20}$$

$$H_{c3} + H_{c2} + H_{c1} = 1. \tag{4.21}$$

There are six equations (4.16) through (4.21) and 9 unknowns (H_{a3}, H_{b3}, H_{c3}…H_{c1}). The set of equations has an indeterminate solution. Hence an optimization technique is used to find the solution of the equations. This solution is for the minimization of the sum of the squares of the switching functions. Equivalently, this is the maximization of the inverter output-input voltage gain

$$\sum K_1 H_{a3}^{\ 2} + K_2 H_{a2}^{\ 2} + K_3 H_{a1}^{\ 2} + K_4 H_{b3}^{\ 2} + K_5 H_{b2}^{\ 2} + K_6 H_{b1}^{\ 2} + K_7 H_{c3}^{\ 2} + K_8 H_{c2}^{\ 2} + K_9 H_{c1}^{\ 2}$$
- Objective Function (4.22)

where $K_{1\text{-}9}$ are sharing functions.

The above objective function has to be minimized subject to the six constraint equations mentioned above.

Writing the six equations in the matrix form,

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \\ 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} V_3 & V_2 & V_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & V_3 & V_2 & V_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & V_3 & V_2 & V_1 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} H_{a3} \\ H_{a2} \\ H_{a1} \\ H_{b3} \\ H_{b2} \\ H_{b1} \\ H_{c3} \\ H_{c2} \\ H_{c1} \end{bmatrix}. \qquad (4.23)$$

In view of this indeterminacy, there are an infinite number of solutions, which are obtained by various optimizing performance functions defined in terms of the modulation functions. For a set of linear indeterminate equations expressed as AX = Y, a solution which minimizes the sum of squares of the variable X is obtained using the Moore-Penrose inverse [84].

From the matrix properties if A is a matrix of rank (r x n) then the product form $A^T A$ has the dimension (n x n) while the product AA^T has dimension of (r x r). If r > n, then $A^T A$ could be nonsingular but AA^T is a singular matrix. Similarly if r < n, AA^T can be a nonsingular matrix but $A^T A$ is a singular matrix. The solution of under-determined case in which the dimension of the matrix A (r x n) where r < n has the matrix A particularly simple transformation is used when rescaling a vector. For example, the original n-vector is X_1, while the desired n-vector is X_2. The vector is rescaled with the diagonal matrix D, whose nonzero elements are the necessary conversion factors:

$$X_2 = D\, X_1. \tag{4.24}$$

By definition, D^{-1} exists, so D is "one-to-one" and "onto," allowing X_1 to be uniquely determined from X_2, and vice versa.

Expressing the r-vector Y as a function of X_2,

$$\begin{aligned} Y &= A_1\, D^{-1}\, X_2 \\ &= A_2\, X_2. \end{aligned} \tag{4.25}$$

Suppose that r < n, and the inverse relationship between X_2 and Y is desired. The right pseudoinverse solution is

$$\begin{aligned} X_2 &= A_2{}^R\, Y \\ &= A_2{}^T\, (A_2\, A_2{}^T)^{-1}\, Y. \end{aligned} \tag{4.26}$$

This is the minimum norm solution for X_2. The corresponding X_1 solution can be found by substitution. Substituting Eq. (4.26) to Eq. (4.25), noting that $D = D^T$ and $D^{-1} = (D^{-1})^T = D^{-T}$

$$\begin{aligned} X_1 &= D^{-1}\, X_2 \\ &= D^{-1}\, A_2{}^R\, Y \\ &= D^{-1}[D^{-1}\, A_1{}^T\, (A_1\, D^{-1}\, D^{-1}\, A_1{}^T)^{-1}]\, Y \\ &= Z^{-1} A_1{}^T (A_1\, Z^{-1}\, A_1{}^T)^{-1}\, Y \end{aligned}$$

where the diagonal matrix Z

$$Z = \begin{bmatrix} \frac{1}{K_1} & 0 & 0 & \dots & 0 \\ 0 & \frac{1}{K_2} & 0 & \dots & 0 \\ . & . & . & . & . \\ . & . & . & . & . \\ 0 & 0 & 0 & 0 & \frac{1}{K_{3N}} \end{bmatrix}.$$

The optimized solution of the matrix (4.19) is given by

$$X = Z\,A^{T}\,[A\,Z\,A^{T}]^{-1}\,Y. \tag{4.27}$$

where Z is given by

$$\begin{bmatrix}
\frac{1}{K_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{K_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{K_3} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{K_4} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{K_5} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{K_6} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_7} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_8} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_9}
\end{bmatrix}.$$

In the present case consider

$$K_1 = K_4 = K_7$$

$$K_2 = K_5 = K_8$$

$$K_3 = K_6 = K_9.$$

In the above mentioned assumption, say $K_1 = K_4 = K_7$, it states that the sharing function corresponding to the top devices in all the three phases is equal and correspondingly the remaining assumptions are for the other devices.

Hence the solution to the objective function gives the expressions for the switching functions.

$$H_{a3} = \frac{v_{a0}V_3K_3 + V_{a0}V_3K_2 - v_{a0}V_2K_3 - v_{a0}V_1K_2 - V_3V_2K_3 - V_1V_3K_2 + {V_2}^2K_3 + {V_1}^2K_2}{\Delta}$$

$$H_{a2} = \frac{v_{a0}V_2K_3 + v_{a0}V_3K_1 - v_{a0}V_3K_3 - v_{a0}V_1K_1 - V_3V_2K_3 - V_1V_2K_1 + {V_3}^2K_3 + {V_1}^2K_1}{\Delta}$$

$$H_{a1} = \frac{v_{a0}V_1K_2 + v_{a0}V_1K_1 - v_{a0}V_3K_2 - v_{a0}V_2K_1 - V_3V_1K_2 - V_2V_1K_1 + {V_3}^2K_2 + {V_1}^2K_2}{\Delta}$$

$$H_{b3} = \frac{v_{b0}V_3K_3 + v_{b0}V_3K_2 - v_{b0}V_2K_3 - v_{b0}V_1K_2 - V_3V_2K_3 - V_1V_3K_2 + {V_2}^2K_3 + {V_1}^2K_2}{\Delta}$$

$$H_{b2} = \frac{v_{b0}V_2K_3 + v_{b0}V_3K_1 - v_{b0}V_3K_3 - v_{b0}V_1K_1 - V_3V_2K_3 - V_1V_2K_1 + {V_3}^2K_3 + {V_1}^2K_1}{\Delta}$$

$$H_{b1} = \frac{v_{b0}V_1K_2 + v_{b0}V_1K_1 - v_{b0}V_3K_2 - v_{b0}V_2K_1 - V_3V_1K_2 - V_2V_1K_1 + {V_3}^2K_2 + {V_2}^2K_1}{\Delta}$$

$$H_{c3} = \frac{v_{c0}V_3K_3 + v_{c0}V_3K_2 - v_{c0}V_2K_3 - v_{c0}V_1K_2 - V_3V_2K_3 - V_1V_3K_2 + {V_2}^2K_3 + {V_1}^2K_2}{\Delta}$$

$$H_{c2} = \frac{v_{c0}V_2K_3 + v_{c0}V_3K_1 - v_{c0}V_3K_3 - v_{c0}V_1K_1 - V_3V_2K_3 - V_1V_2K_1 + {V_3}^2K_3 + {V_1}^2K_1}{\Delta}$$

$$H_{c1} = \frac{v_{c0}V_1K_2 + v_{c0}V_1K_1 - v_{c0}V_3K_2 - v_{c0}V_2K_1 - V_3V_1K_2 - V_2V_1K_1 + {V_3}^2K_2 + {V_1}^2K_2}{\Delta}$$

(4.27-4.35)

where

$$\Delta = {V_3}^2K_6 + {V_3}^2K_5 + {V_2}^2K_6 + {V_2}^2K_4 + {V_1}^2K_5 + {V_1}^2K_4 - 2V_3K_6V_2 - 2V_3K_5V_1 - 2V_2K_4V_1.$$

Under balanced conditions the steady state values of the node voltages are

$$V_3 = \frac{V_d}{2}$$
$$V_2 = 0$$
$$V_1 = \frac{-V_d}{2}.$$

Hence by substituting the above steady state values and assuming all the sharing functions to be equal to be unity in Eqs. (4.27 - 4.35)

$$H_{a3} = \frac{2v_{a0}}{3V_d} + \frac{1}{3} \qquad H_{b3} = \frac{2v_{b0}}{3V_d} + \frac{1}{3} \qquad H_{c3} = \frac{2v_{c0}}{3V_d} + \frac{1}{3} \tag{4.36}$$

$$H_{a2} = \frac{1}{3} \qquad H_{b2} = \frac{1}{3} \qquad H_{c2} = \frac{1}{3} \tag{4.37}$$

$$H_{a1} = -\frac{2v_{a0}}{3V_d} + \frac{1}{3} \qquad H_{b1} = -\frac{2v_{b0}}{3V_d} + \frac{1}{3} \qquad H_{c1} = -\frac{2v_{c0}}{3V_d} + \frac{1}{3}. \tag{4.38}$$

The pattern of switching for the switching devices used in converter is periodic; therefore the analysis of the switching functions is simple by using the Fourier series. Thus the switching pulses can be represented as sum of dc component and fundamental component either sine or cosine varying term. It can be assumed as

$$H_{a3} = \frac{1}{3}\left(1 + M_{a3}\right) \tag{4.39}$$

$$H_{a2} = \frac{1}{3}\left(1 + M_{a2}\right) \tag{4.40}$$

$$H_{a1} = \frac{1}{3}\left(1 + M_{a1}\right) \tag{4.41}$$

where M_{a3}, M_{a2}, M_{a1} are called the modulation signals, which can be cosine or sine term. These signals represent the fundamental component of the switching pulses. When this fundamental component is compared with the high frequency carrier waveform produces the same pattern of the pulses.

By comparing Eqs. (4.39 – 4.41) with Eqs. (4.36 – 4.38), the modulation signals are obtained as

$$M_{a3} = \frac{2v_{a0}}{V_d}\ ,\ M_{a2} = 0\ ,\ M_{a3} = \frac{-2v_{a0}}{V_d}\ . \tag{4.42}$$

The modulation signals for the top and the bottom devices are exactly in opposite in phase and this can be seen in Figure 4.2.

The node currents of the inverter are given by

$$I_3 = H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{4.43}$$

$$I_2 = H_{a2} i_a + H_{b2} i_b + H_{c2} i_c \tag{4.44}$$

$$I_1 = H_{a1} i_a + H_{b1} i_b + H_{c1} i_c . \tag{4.45}$$

Writing the KCL equation at node 3 gives the differential equation of the capacitor voltage V_{c1} and KCL equation at node 1 gives differential equation for capacitor voltage V_{c2}.

$$C_1 p V_{c1} = -I_{dc} + H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{4.46}$$

$$C_2 p V_{c2} = -\left(I_{dc} + H_{a1} i_a + H_{b1} i_b + H_{c1} i_c\right) \tag{4.47}$$

Figure 4.2 shows the carrier-based PWM technique where three modulation signals are compared with the carrier waveform.

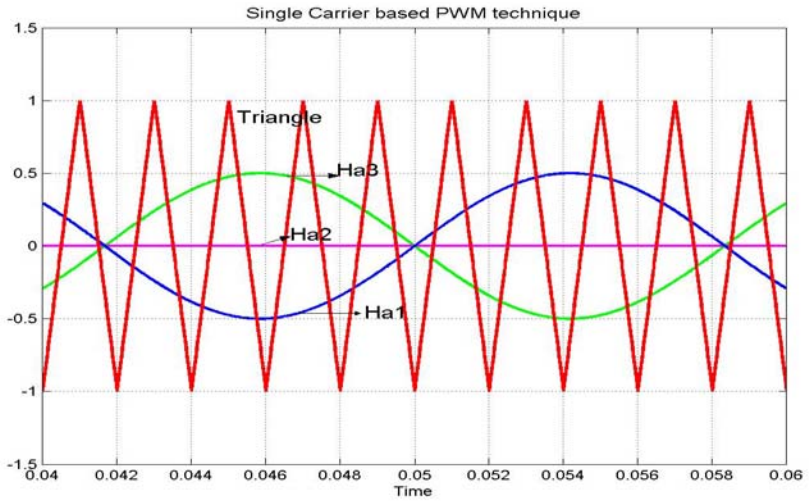


Figure 4.2: Single carrier and multiple modulation signal PWM technique for a three-level inverter.

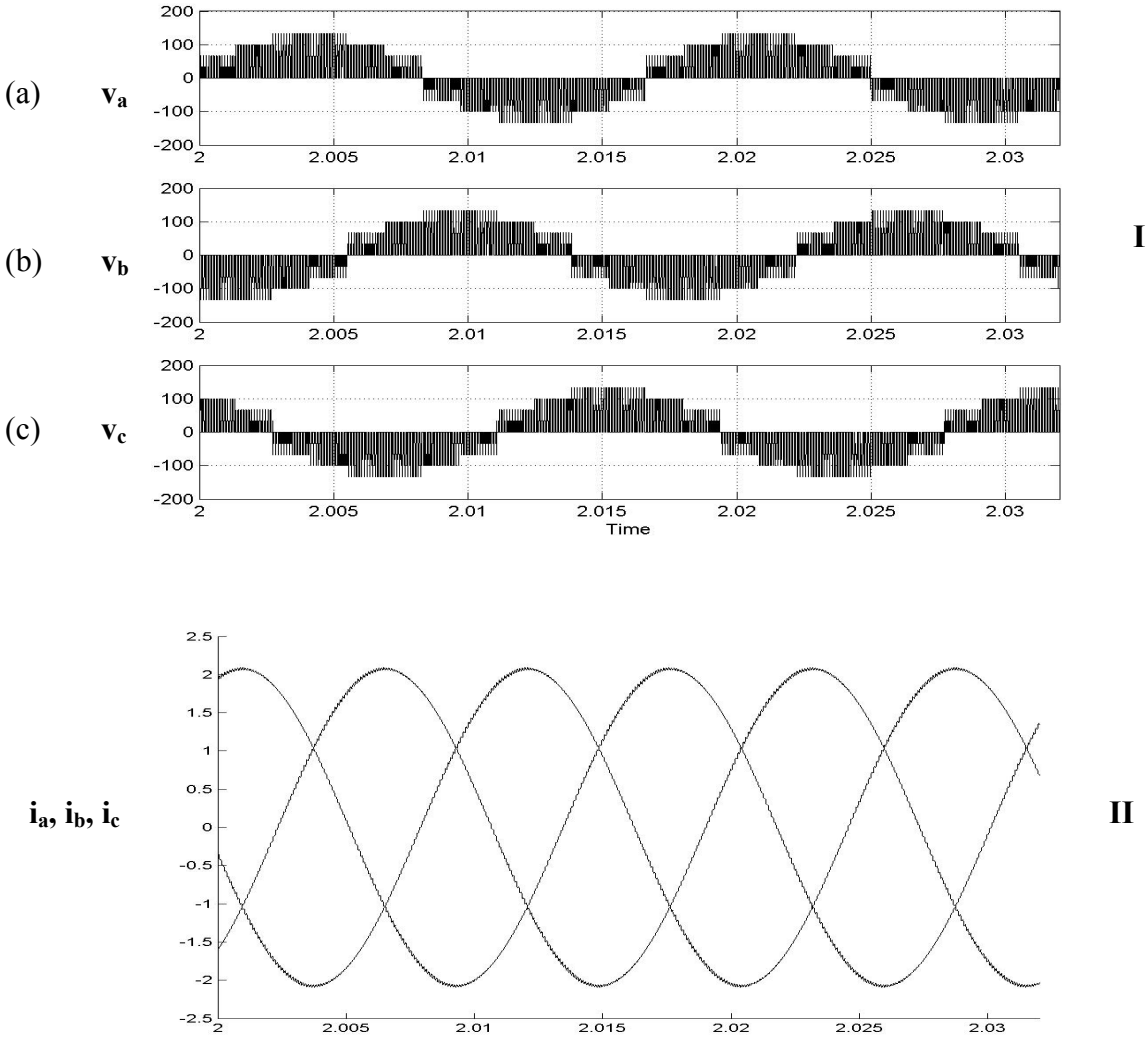


Figure 4.3: Simulation results of three-level inverter using the single carrier-based technique (I) (a), (b), (c) Three-phase voltages (II) three-phase currents

Using the modulation signals that are obtained using Eq. (4.42), the carrier-based PWM is implemented. Figure 4.3 illustrates the simulation results for a three-level inverter, which is modulated using the single carrier-based PWM technique. Figure 4.3 (I) (a), (b), (c) shows the three-phase voltages generated. Figure 4.3 (II) gives the three-phase currents generated when the voltages are impressed across a balanced three-phase load.

4.3.2 Four-Level Inverter

The output voltages of the four-level inverter is defined by the following equations.

$$v_{ao} = H_{a4}V_{40} + H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10} \tag{4.48}$$

$$v_{bo} = H_{b4}V_{40} + H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10} \tag{4.49}$$

$$v_{co} = H_{c4}V_{40} + H_{c3}V_{30} + H_{c2}V_{20} + H_{c1}V_{10} \tag{4.50}$$

The switching constraints to be followed in order to avoid the shorting of the dc bus voltage source are

$$H_{a4} + H_{a3} + H_{a2} + H_{a1} = 1 \tag{4.51}$$

$$H_{b4} + H_{b3} + H_{b2} + H_{b1} = 1 \tag{4.52}$$

$$H_{c4} + H_{c3} + H_{c2} + H_{c1} = 1. \tag{4.53}$$

There are six equations and 12 unknowns (H_{a4}, H_{b4}, H_{c4} … H_{c1}), the set of equations has an indeterminate solution. The optimization technique used in case of three-level is extended to four-level to obtain the solution, which minimizes the sum of the squares of the switching functions. Equivalently, this is the maximization of the inverter output-input voltage gain

$$\sum \begin{pmatrix} K_1 H_{a4}^{\ 2} + K_2 H_{a3}^{\ 2} + K_3 H_{a2}^{\ 2} + K_4 H_{a1}^{\ 2} + K_5 H_{b4}^{\ 2} + K_6 H_{b3}^{\ 2} + K_7 H_{b2}^{\ 2} + K_8 H_{b1}^{\ 2} + K_9 H_{c4}^{\ 2} \\ \\ + K_{10} H_{c3}^{\ 2} + K_{11} H_{c2}^{\ 2} + K_{12} H_{c1}^{\ 2} \end{pmatrix}$$

- Objective Function. (4.54)

Hence the above objective function has to be minimized subject to six constraint equations mentioned above.

Writing the six equations in the matrix form,

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \\ 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} V_4 & V_3 & V_2 & V_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & V_4 & V_3 & V_2 & V_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & V_4 & V_3 & V_2 & V_1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} H_{a4} \\ H_{a3} \\ H_{a2} \\ H_{a1} \\ H_{b4} \\ H_{b3} \\ H_{b2} \\ H_{b1} \\ H_{c4} \\ H_{c3} \\ H_{c2} \\ H_{c1} \end{bmatrix} \tag{4.55}$$

Under balanced conditions the steady state values of the node voltages are

$$V_4 = \frac{V_d}{2}$$
$$V_3 = \frac{V_d}{6}$$
$$V_2 = -\frac{V_d}{6}$$
$$V_1 = \frac{-V_d}{2}.$$

The above matrix is in the form of Y = A X.

The optimized solution of the above matrix is given by

$$X = Z\, A^T\, [A\, Z\, A^T]^{-1}\, Y$$

where Z is given by

$$\begin{bmatrix}
\frac{1}{K_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{K_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{K_3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{K_4} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{K_5} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{K_6} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_7} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_8} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_9} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{10}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{11}} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{12}}
\end{bmatrix}.$$

Assuming the following,

$$K_1 = K_5 = K_9$$

$$K_2 = K_6 = K_{10}$$

$$K_3 = K_7 = K_{11}$$

$$K_4 = K_8 = K_{12}.$$

By substituting the above assumption and solving the matrix gives the expressions for the modulation signals [A.1]. The steady state modulation signals are obtained by substituting the steady-state values of the node voltages and sharing function to be unity in [A.1],

$$H_{a4} = \frac{3v_{a0}}{4V_d} + \frac{1}{4} \qquad H_{b4} = \frac{3v_{b0}}{4V_d} + \frac{1}{4} \qquad H_{c4} = \frac{3v_{c0}}{4V_d} + \frac{1}{4} \tag{4.56}$$

$$H_{a3} = \frac{v_{a0}}{4V_d} + \frac{1}{4} \qquad H_{b3} = \frac{v_{b0}}{4V_d} + \frac{1}{4} \qquad H_{c3} = \frac{v_{c0}}{4V_d} + \frac{1}{4} \tag{4.57}$$

$$H_{a2} = -\frac{v_{a0}}{4V_d} + \frac{1}{4} \qquad H_{b2} = -\frac{v_{b0}}{4V_d} + \frac{1}{4} \qquad H_{c2} = -\frac{v_{c0}}{4V_d} + \frac{1}{4} \tag{4.58}$$

$$H_{a1} = -\frac{3v_{a0}}{4V_d} + \frac{1}{4} \qquad H_{b1} = -\frac{v_{b0}}{4V_d} + \frac{1}{4} \qquad H_{c1} = -\frac{3v_{c0}}{4V_d} + \frac{1}{4}. \tag{4.59}$$

Similarly representing the switching pulses as sum of dc component and fundamental component either sine or cosine varying term.

$$H_{a4} = \frac{1}{4}\left(1 + M_{a4}\right) \tag{4.60}$$

$$H_{a3} = \frac{1}{4}\left(1 + M_{a3}\right) \tag{4.61}$$

$$H_{a2} = \frac{1}{4}\left(1 + M_{a2}\right) \tag{4.62}$$

$$H_{a1} = \frac{1}{4}\left(1 + M_{a1}\right) \tag{4.63}$$

Comparing the switching functions in Eqs. (4.56 – 4.59) and Eqs. (4.60 – 4.63)

$$M_{a4} = \frac{3v_{a0}}{V_d},\ M_{a3} = \frac{v_{a0}}{V_d},\ M_{a2} = -\frac{v_{a0}}{V_d},\ M_{a1} = \frac{-3v_{a0}}{V_d}. \tag{4.64}$$

Figure 4.4 shows the single carrier and multiple modulation signal technique for a four-level inverter. The relation between the modulation signals is that two modulation signals (H_{a4}, H_{a3}) are in phase and (H_{a2}, H_{a1}) are in phase and these two combinations are exactly opposite in phase.

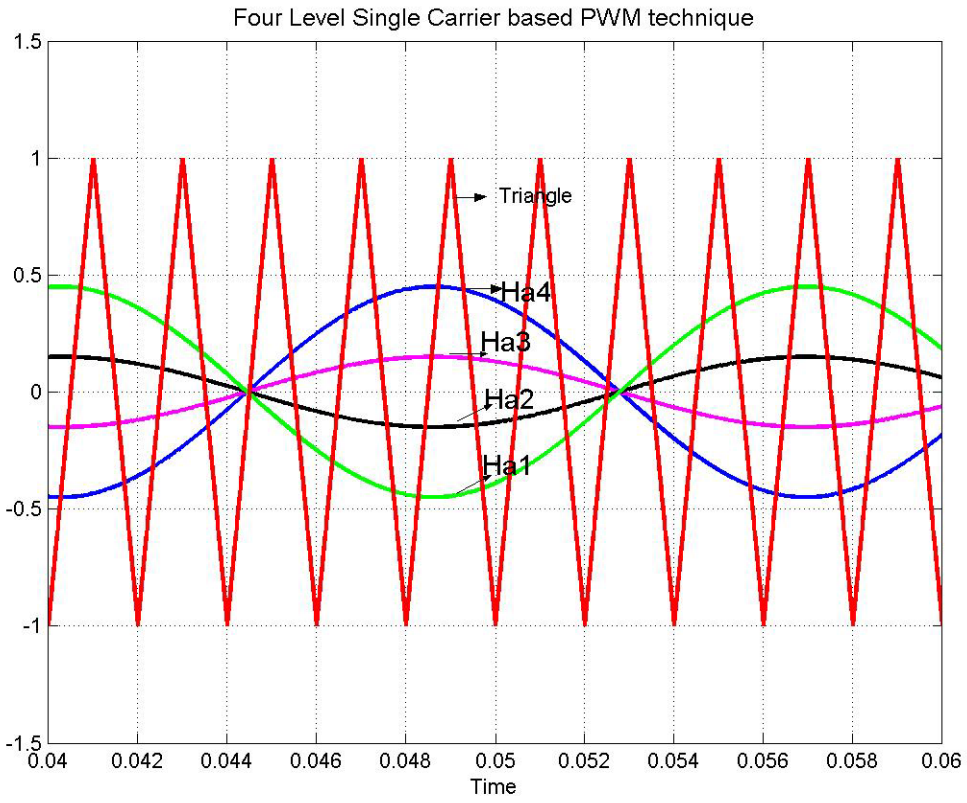


Figure 4.4: Single Carrier and Multiple Modulation Signal PWM Technique for a Four-Level Inverter.

The node currents of the inverter are given by

$$I_4 = H_{a4} i_a + H_{b4} i_b + H_{c4} i_c \tag{4.65}$$

$$I_3 = H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{4.66}$$

$$I_2 = H_{a2} i_a + H_{b2} i_b + H_{c2} i_c \tag{4.67}$$

$$I_1 = H_{a1} i_a + H_{b1} i_b + H_{c1} i_c . \tag{4.68}$$

Writing the KCL equation at node 4 gives the differential equation of the capacitor voltage V_{c1}, KCL equation at node 3 gives differential equation for capacitor voltage V_{c2}, and KCL equation at node 2 gives differential equation for capacitor voltage V_{c1}.

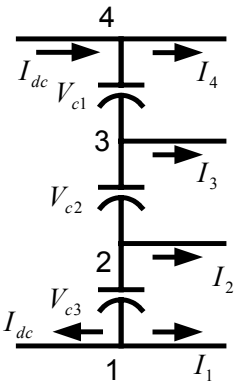


Figure 4.5: Schematic of a Four Level Inverter.

$$C_1 pV_{c1} = I_{dc} - H_{a4} i_a - H_{b4} i_b - H_{c4} i_c \tag{4.69}$$

$$C_2 pV_{c2} = \left(I_{dc} - H_{a4} i_a - H_{b4} i_b - H_{c4} i_c - H_{a3} i_a - H_{b3} i_b - H_{c3} i_c\right) \tag{4.70}$$

$$C_3 pV_{c3} = \left(I_{dc} - H_{a4} i_a - H_{b4} i_b - H_{c4} i_c - H_{a3} i_a - H_{b3} i_b - H_{c3} i_c - H_{a2} i_a - H_{b2} i_b - H_{c2} i_c\right) \tag{4.71}$$

4.3.3 Five-Level Inverter

The output voltages of the five-level inverter are defined by the following equations.

$$v_{ao} = H_{a5} V_{50} + H_{a4} V_{40} + H_{a3} V_{30} + H_{a2} V_{20} + H_{a1} V_{10} \tag{4.72}$$

$$v_{bo} = H_{b5} V_{50} + H_{b4} V_{40} + H_{b3} V_{30} + H_{b2} V_{20} + H_{b1} V_{10} \tag{4.73}$$

$$v_{co} = H_{c5} V_{50} + H_{c4} V_{40} + H_{c3} V_{30} + H_{c2} V_{20} + H_{c1} V_{10}\,. \tag{4.74}$$

The switching constraints to be followed in order to avoid the shorting of the dc bus voltage source are

$$H_{a5} + H_{a4} + H_{a3} + H_{a2} + H_{a1} = 1 \tag{4.75}$$

$$H_{b5} + H_{b4} + H_{b3} + H_{b2} + H_{b1} = 1 \tag{4.76}$$

$$H_{c5} + H_{c4} + H_{c3} + H_{c2} + H_{c1} = 1. \tag{4.77}$$

There are six equations and fifteen unknowns (H_{a5}, H_{c5}, H_{b5} … H_{c1}); the set of equations has an indeterminate solution. Optimization technique is used to obtain the solution, which minimizes the sum of the squares of the switching functions. Equivalently, this is the maximization of the inverter output-input voltage gain

$$\sum \begin{pmatrix} K_1 H_{a5}{}^2 + K_2 H_{a4}{}^2 + K_3 H_{a3}{}^2 + K_4 H_{a2}{}^2 + K_5 H_{a1}{}^2 + K_6 H_{b5}{}^2 + K_7 H_{b4}{}^2 + K_8 H_{b3}{}^2 + K_9 H_{b2}{}^2 \\ + K_{10} H_{b1}{}^2 + K_{11} H_{c5}{}^2 + K_{12} H_{c4}{}^2 + K_{13} H_{c3}{}^2 + K_{14} H_{c2}{}^2 + K_{15} H_{c1}{}^2. \end{pmatrix}$$

- Objective Function. (4.78)

Under balanced conditions the steady state values of the node voltages are

$$V_5 = \frac{V_d}{2};\ V_4 = \frac{V_d}{4};\ V_3 = 0;\ V_2 = -\frac{V_d}{4};\ V_1 = \frac{-V_d}{2}.$$

Representing Eqs. (4.72 – 4.77) in the matrix form as follows.

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \\ 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} V_5 & V_4 & V_3 & V_2 & V_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & V_5 & V_4 & V_3 & V_2 & V_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & V_5 & V_4 & V_3 & V_2 & V_1 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} H_{a5} \\ H_{a4} \\ H_{a3} \\ H_{a2} \\ H_{a1} \\ H_{b5} \\ H_{b4} \\ H_{b3} \\ H_{b2} \\ H_{b1} \\ H_{c5} \\ H_{c4} \\ H_{c3} \\ H_{c2} \\ H_{c1} \end{bmatrix}$$

The above matrix is in the form of Y = A X.

The optimized solution of the above matrix is given by

$$X = Z\,A^{T}\,[A\,Z\,A^{T}]^{-1}\,Y$$

where Z is given by

$$Z = \begin{bmatrix}
\frac{1}{K_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{K_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{K_3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{K_4} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{K_5} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{K_6} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_7} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_8} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_9} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{10}} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{11}} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{12}} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{13}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{14}} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_{15}}
\end{bmatrix}$$

Assuming the following,

$$K_1 = K_6 = K_{11}$$

$$K_2 = K_7 = K_{12}$$

$$K_3 = K_8 = K_{13}$$

$$K_4 = K_9 = K_{14}$$

$$K_5 = K_{10} = K_{15}.$$

By substituting the above assumption and solving the matrix gives the expressions for the modulation signals [A.2]. Substituting the above steady state values and assuming all the sharing functions to be equal to be unity, the modulation signals are obtained as

$$H_{a5} = \frac{4v_{a0}}{5V_d} + \frac{1}{5} \qquad H_{b5} = \frac{4v_{b0}}{5V_d} + \frac{1}{5} \qquad H_{c5} = \frac{4v_{c0}}{5V_d} + \frac{1}{5} \tag{4.79}$$

$$H_{a4} = \frac{2v_{a0}}{5V_d} + \frac{1}{5} \qquad H_{b4} = \frac{2v_{b0}}{5V_d} + \frac{1}{5} \qquad H_{c4} = \frac{2v_{c0}}{5V_d} + \frac{1}{5} \tag{4.80}$$

$$H_{a3} = \frac{1}{5} \qquad H_{b3} = \frac{1}{5} \qquad H_{b3} = \frac{1}{5} \tag{4.81}$$

$$H_{a2} = -\frac{2v_{a0}}{5V_d} + \frac{1}{5} \qquad H_{b2} = -\frac{2v_{b0}}{5V_d} + \frac{1}{5} \qquad H_{c2} = -\frac{2v_{c0}}{5V_d} + \frac{1}{5} \tag{4.82}$$

$$H_{a1} = -\frac{4v_{a0}}{5V_d} + \frac{1}{5} \qquad H_{b1} = -\frac{4v_{b0}}{5V_d} + \frac{1}{5} \qquad H_{c1} = -\frac{4v_{c0}}{5V_d} + \frac{1}{5}. \tag{4.83}$$

The modulation signals are obtained by comparing the switching pulses with the Fourier series approximation,

$$H_{a5} = \frac{1}{5}\left(1 + M_{a5}\right) \tag{4.84}$$

$$H_{a4} = \frac{1}{5}\left(1 + M_{a4}\right) \tag{4.85}$$

$$H_{a3} = \frac{1}{5}\left(1 + M_{a3}\right) \tag{4.86}$$

$$H_{a2} = \frac{1}{5}\left(1 + M_{a2}\right) \tag{4.87}$$

$$H_{a1} = \frac{1}{5}\left(1 + M_{a1}\right). \tag{4.88}$$

By comparing the switching functions in Eqs. (4.79 – 4.83) with Eqs. (4.84 – 4.88), the modulation signals are obtained as

$$M_{a5} = \frac{4v_{a0}}{V_d}\ ,\ M_{a4} = \frac{2v_{a0}}{V_d}, M_{a3} = 0\,,\ M_{a2} = -\frac{2v_{a0}}{V_d}\,,\ M_{a1} = \frac{-4v_{a0}}{V_d}\,. \tag{4.89}$$

The above equation gives the modulation signals for phase "a." Similarly the modulation signals for the other phase can be obtained. In case of five level inverter, the modulation signal of the top two devices are in phase and exactly opposite in phase with the bottom two devices. The signal corresponding to the neutral point is zero.

4.3.4 Generalization of the Modulation Scheme for N-level Inverters

Consider a general N level multilevel inverter, in which the inverter has N-1 dc-link voltages, N node current I_N, I_{N-1},…, I_1, and 3N switching functions for all the three phase H_{aN}, H_{aN-1},…,H_{a1} and similarly for the other phases.

The output phase voltages of the inverter are given by

$$v_{ao} = H_{aN}V_{N0} + H_{aN-1}V_{N-10} + ... + H_{a1}V_{10} \tag{4.90}$$

$$v_{bo} = H_{bN}V_{N0} + H_{bN-1}V_{N-10} + ... + H_{b1}V_{10} \tag{4.91}$$

$$v_{co} = H_{cN}V_{N0} + H_{cN-1}V_{N-10} + ... + H_{c1}V_{10}. \tag{4.92}$$

To avoid the shorting of the leg the following constraint has to be followed

$$H_{aN} + H_{aN-1} + ... + H_{a1} = 1 \tag{4.93}$$

$$H_{bN} + H_{bN-1} + ... + H_{b1} = 1 \tag{4.94}$$

$$H_{cN} + H_{cN-1} + ... + H_{c1} = 1. \tag{4.95}$$

Eqs. (4.62 – 4.67) are solved using the optimization technique explained above.

The optimized solution of the equations is given by

$$\mathrm{X = Z\ A^T\ [\ A\ Z\ A^T\ ]^{-1}\ Y}$$

where

$$Z = \begin{bmatrix} \frac{1}{K_1} & 0 & 0 & ... & 0 \\ 0 & \frac{1}{K_2} & 0 & ... & 0 \\ . & . & . & . & . \\ . & . & . & . & . \\ 0 & 0 & 0 & 0 & \frac{1}{K_{3N}} \end{bmatrix}.$$

The following assumption has to be made

$$K_1 = K_{N+1} = K_{2N+1}$$

$$K_2 = K_{N+2} = K_{2N+2}$$

$$K_3 = K_{N+3} = K_{2N+3}$$

•

•

$$K_N = K_{2N} = K_{3N}.$$

By substituting all the sharing functions to be unity, the switching functions are obtained as

$$H_{aN} = \frac{(N-1)v_{ao}}{NV_d} + \frac{1}{N} \qquad H_{bN} = \frac{(N-1)v_{bo}}{NV_d} + \frac{1}{N} \qquad H_{cN} = \frac{(N-1)v_{co}}{NV_d} + \frac{1}{N}$$

$$H_{aN-1} = \frac{(N-3)v_{ao}}{NV_d} + \frac{1}{N} \qquad H_{bN-1} = \frac{(N-3)v_{bo}}{NV_d} + \frac{1}{N} \qquad H_{cN-1} = \frac{(N-3)v_{co}}{NV_d} + \frac{1}{N}$$

. . .

. . .

$$H_{a1} = \frac{-(N-1)v_{ao}}{NV_d} + \frac{1}{N} \qquad H_{b1} = \frac{-(N-1)v_{bo}}{NV_d} + \frac{1}{N} \qquad H_{c1} = \frac{-(N-1)v_{co}}{NV_d} + \frac{1}{N}.$$

The above equations give the generalized switching functions for a N-level inverter.

Assuming the switching function for a N-level case as

$$H_{aN} = \frac{1}{N}(1 + M_{aN}),\ H_{aN-1} = \frac{1}{N}(1 + M_{aN-1}) \ldots\ H_{a1} = \frac{1}{N}(1 + M_{a1}). \tag{4.96}$$

By comparing the switching function with Eq. (4.96), the modulation are obtained as

$$M_{aN} = \frac{(N-1)v_{ao}}{V_d}$$

$$M_{aN-1} = \frac{(N-3)v_{ao}}{V_d}$$

.

$$M_{a1} = \frac{-(N-1)v_{ao}}{V_d}.$$

The above equations represent the generalized form of the modulation signals for a N-level converter.

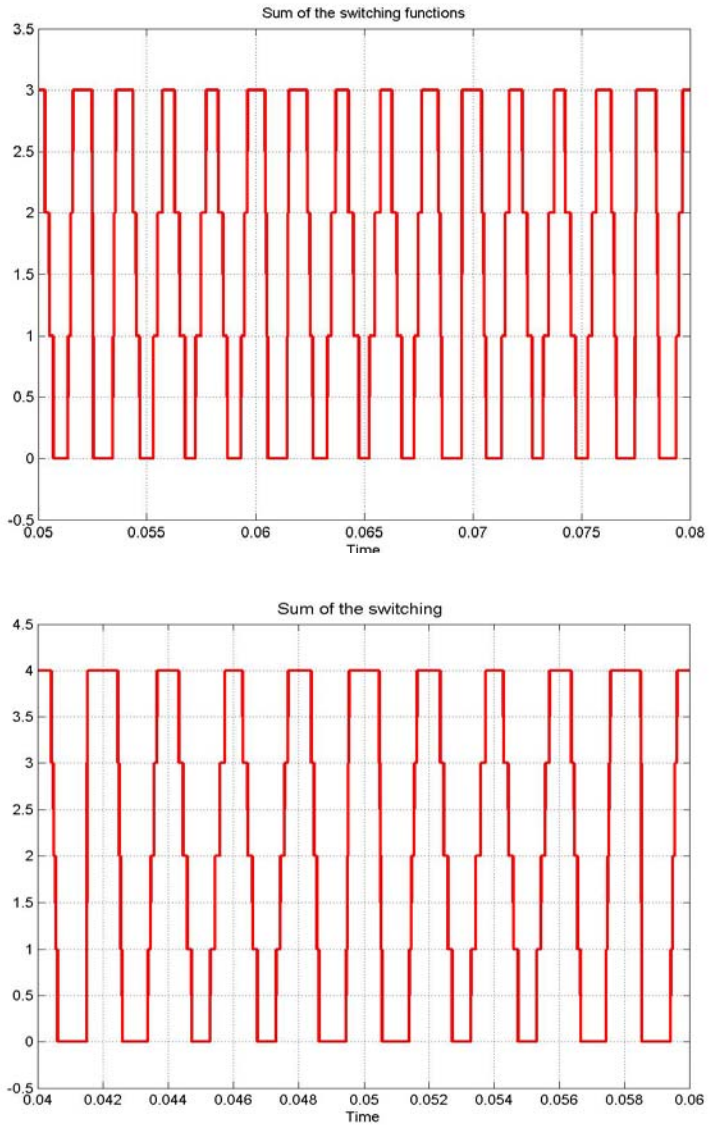


Figure 4.6: Sum of the switching functions (I) Three-level inverter (II) Four-level inverter.

Figure 4.6 (I) and (II) shows the sum of the switching functions produced using the single carrier and multiple modulation signals. As seen from the figure, the sum of the switching functions is not equal to 1; i.e., there is more than one device that is on at a time, which eventually shorts the input dc capacitors. The shorting of the devices is inherent and can only be avoided using logic. Hence this is a major drawback of the scheme.

There some limitations in the scheme proposed:

- There is shorting between the devices of the leg; i.e., the input side capacitors are getting shorted which is not acceptable.
- Every time the voltage switches from zero to the node voltage it is connected and hence the entire voltage is impressed across the devices and hence high rating devices have to be used.

4.4 Equivalence of Two-Triangle Method and Single Triangle Method

The main drawback of the single carrier-based method was the shorting problem; to overcome this problem, the conventional (N-1) carrier waveforms and single modulation signal is used. In this section, the equivalence of the single carrier and multiple carrier-based PWM technique is presented.

The output voltage of a three-level inverter is given by

$$H_{a3}V_{c1} - H_{a1}V_{c2} = V_{a0} + V_{02} \tag{4.97}$$

$$H_{b3}V_{c1} - H_{b1}V_{c2} = V_{b0} + V_{02} \tag{4.98}$$

$$H_{c3}V_{c1} - H_{c1}V_{c2} = V_{c0} + V_{02}. \tag{4.99}$$

Transforming the above equation to synchronous reference frame by using transformation matrix $T(\theta)$, where

$$T(\theta)=\frac{2}{3}\begin{bmatrix}\cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3})\\ \sin(\theta) & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3})\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix} \tag{4.100}$$

$\theta=\int \omega_e dt+\theta_0$; θ_0 - Initial reference angle.

The qd equations are obtained as

$$V_q^{\ e}=V_{c1}H_{q3}-V_{c2}H_{q1} \tag{4.101}$$

$$V_d^{\ e}=V_{c1}H_{d3}-V_{c2}H_{d1} \tag{4.102}$$

$$V_0^{\ e}=V_{c1}H_{03}-V_{c2}H_{01}+V_{02} \tag{4.103}$$

where

$$H_{q3}=\frac{2}{3}\left[H_{a3}\cos(\theta)+H_{b3}\cos(\theta-\frac{2\pi}{3})+H_{c3}\cos(\theta+\frac{2\pi}{3})\right] \tag{4.104}$$

$$H_{d3}=\frac{2}{3}\left[H_{a3}\sin(\theta)+H_{b3}\sin(\theta-\frac{2\pi}{3})+H_{c3}\sin(\theta+\frac{2\pi}{3})\right] \tag{4.105}$$

$$H_{03}=\frac{1}{3}\left[H_{a3}+H_{b3}+H_{c3}\right]. \tag{4.106}$$

Similarly

$$H_{q1}=\frac{2}{3}\left[H_{a1}\cos(\theta)+H_{b1}\cos(\theta-\frac{2\pi}{3})+H_{c1}\cos(\theta+\frac{2\pi}{3})\right] \tag{4.107}$$

$$H_{d1}=\frac{2}{3}\left[H_{a1}\sin(\theta)+H_{b1}\sin(\theta-\frac{2\pi}{3})+H_{c1}\sin(\theta+\frac{2\pi}{3})\right] \tag{4.108}$$

$$H_{01}=\frac{1}{3}\left[H_{a1}+H_{b1}+H_{c1}\right]. \tag{4.109}$$

Consider Eqs. (4.101) and (4.102), the LHS can be modified as

$$V_d\ \sigma_q^{'} = V_{c1} H_{q3} - V_{c2} H_{q1} \tag{4.110}$$

$$V_d\ \sigma_d^{'} = V_{c1} H_{d3} - V_{c2} H_{d1}. \tag{4.111}$$

Assuming

$$H_{q3} = \alpha\ H_q\ ;\ H_{q1} = -\beta\ H_q \tag{4.112}$$

$$H_{d3} = \alpha\ H_d\ ;\ H_{d1} = -\beta\ H_d \tag{4.113}$$

α, β are control variables.

Substituting the above condition in Eqs. (4.110) and (4.111), and solving for H_q and H_d

$$H_q = \frac{V_d\ \sigma_q^{'}}{\alpha\ V_{c1} + \beta\ V_{c2}} \tag{4.114}$$

$$H_d = \frac{V_d\ \sigma_d^{'}}{\alpha\ V_{c1} + \beta\ V_{c2}}. \tag{4.115}$$

Substituting Eqs. (4.114) and (4.115) in Eqs. (4.112) and (4.113)

$$H_{q3} = \frac{\alpha\ V_d\ \sigma_q^{'}}{\alpha\ V_{c1} + \beta\ V_{c2}} \qquad H_{q1} = \frac{-\beta\ V_d\ \sigma_q^{'}}{\alpha\ V_{c1} + \beta\ V_{c2}} \tag{4.116}$$

$$H_{d3} = \frac{\alpha\ V_d\ \sigma_d^{'}}{\alpha\ V_{c1} + \beta\ V_{c2}} \qquad H_{d1} = \frac{-\beta\ V_d\ \sigma_d^{'}}{\alpha\ V_{c1} + \beta\ V_{c2}}. \tag{4.117}$$

To obtain the modulation signals in abc reference frame, the qd modulation signals are transformed using the inverse transformation matrix $T^{-1}(\theta)$ back to the abc reference frame, where

$$T^{-1}(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix}. \tag{4.118}$$

The modulation signals are obtained as

$$H_{a3} = \frac{\alpha V_d}{\alpha V_{c1} + \beta V_{c2}} \left[\sigma_q \cos(\theta) + \sigma_d \sin(\theta)\right] + H_{o3} \tag{4.119}$$

$$H_{b3} = \frac{\alpha V_d}{\alpha V_{c1} + \beta V_{c2}} \left[\sigma_q \cos(\theta - \frac{2\pi}{3}) + \sigma_d \sin(\theta - \frac{2\pi}{3})\right] + H_{o3} \tag{4.120}$$

$$H_{c3} = \frac{\alpha V_d}{\alpha V_{c1} + \beta V_{c2}} \left[\sigma_q \cos(\theta + \frac{2\pi}{3}) + \sigma_d \sin(\theta + \frac{2\pi}{3})\right] + H_{o3} \tag{4.121}$$

$$H_{a1} = \frac{-\beta V_d}{\alpha V_{c1} + \beta V_{c2}} \left[\sigma_q \cos(\theta) + \sigma_d \sin(\theta)\right] + H_{o3} \tag{4.122}$$

$$H_{b1} = \frac{-\beta V_d}{\alpha V_{c1} + \beta V_{c2}} \left[\sigma_q \cos(\theta - \frac{2\pi}{3}) + \sigma_d \sin(\theta - \frac{2\pi}{3})\right] + H_{o1} \tag{4.123}$$

$$H_{c1} = \frac{-\beta V_d}{\alpha V_{c1} + \beta V_{c2}} \left[\sigma_q \cos(\theta + \frac{2\pi}{3}) + \sigma_d \sin(\theta + \frac{2\pi}{3})\right] + H_{o1} \tag{4.124}$$

$$H_{a2} = 1 - H_{a1} - H_{a3} \tag{4.125}$$

$$H_{b2} = 1 - H_{b1} - H_{b3} \tag{4.126}$$

$$H_{c2} = 1 - H_{c1} - H_{c3}\,. \tag{4.127}$$

Assuming

$$X = \frac{\alpha V_d}{\alpha V_{c1} + \beta V_{c2}} \text{ and } Y = \frac{-\beta V_d}{\alpha V_{c1} + \beta V_{c2}} \tag{4.128}$$

where X and Y are the modulation indices of the signals in Eqs. (4.119) and (4.122).

In case of two triangle carrier-based technique, α, β decides the peaks of the two carriers and the sum of the two control variables must be equal to two; i.e., $\alpha + \beta = 2$. The upper carrier waveform ranges from $[1 - (1-\alpha)]$ and the lower carrier waveform

ranges from $[(1-\alpha)$- (-1)]. Effectively the magnitudes of the carrier waveforms will be α and β, respectively.

By varying the control variables α, β, the modulation index can be controlled in case of multiple modulation signals and in case of multiple carrier waveforms; the peaks of the carrier waveforms can be controlled. Figure 4.7 shows the comparison between the two schemes.

Single Carrier, H_{a4}, H_{a3}, H_{a2}, H_{a1}.

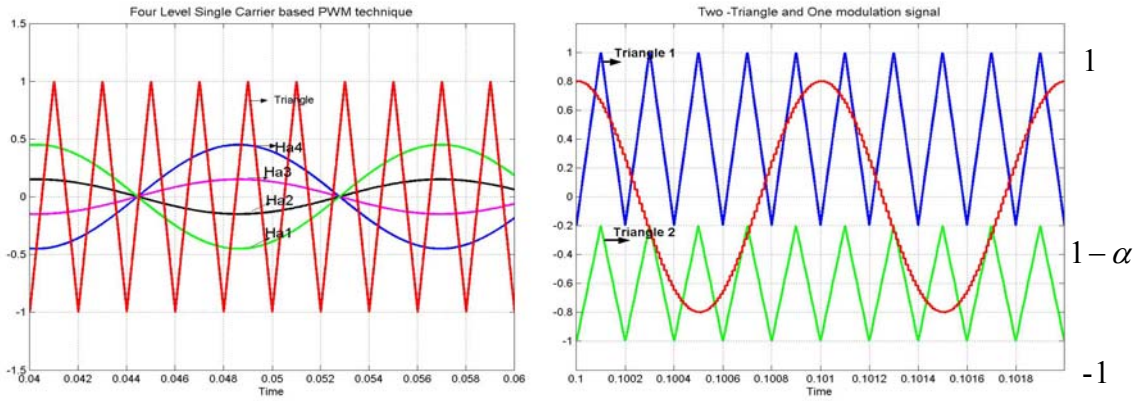


Figure 4.7: Comparison between the Single carrier and multiple carrier waveform PWM methods (I) Single carrier-based PWM (II) Multiple Carrier-based PWM.

Table 4.1: Comparison of single carrier and multiple carrier-based PWM.

	X	Y
$\alpha = 1, \beta = 1$	1	-1
$\alpha = 0, \beta = 2$	0	-2
$\alpha = 2, \beta = 0$	2	0
$\alpha = 0.8, \beta = 1.2$	0.8	-1.2
$\alpha = 1.2, \beta = 0.8$	1.2	-0.8

Table 4. 1 illustrates the relation between the carrier waveform peaks and the modulation signal peaks. Consider $\alpha = 1, \beta = 1$; substituting these values in Eq. (4.128), the modulation indices can be calculated. It can be seen from table 4.1 that the indices are 1 and –1. This is equivalent to the peaks of the triangles in the multiple carrier-based PWM. Similarly for different values of α, β the relation is obtained. It is clear that by varying the modulation signals is equivalent to varying the peaks of the triangle waveforms.

4.5 Space Vector Modulation

4.5.1 Generation of the PWM Switching Signals

It is the task of the modulator to decide which position the switches should assume (switching state), and the duration needed (turn-on time) in order to synthesize the reference voltage vector. In other words, it is the task of the modulator to approximate the reference vector, computed by the controller, using the PWM for several switching vectors. The general space vector can be extended to the multilevel converters; however, the large number of states offered by multilevel converters can impose massive computational overhead if not carefully optimized.

"0" represents that the converter is connected to the negative node voltage, "1" represents that it is connected to the neutral point, and "2" connects the converter to the

positive node voltage. With a three-phase three-level voltage source inverter there are 27 feasible switching modes. Obeying KVL and KCL the generated states are enumerated in Table 4.2. The inverter has 24 active states and three null states. A null state is defined as a state that does not contribute to the generation of the reference voltage. In this state the converter is connected to the same node in all the three phases. By controlling the duty cycles of devices in these zero states, the capacitors can be charged and discharged without contributing to the actual voltage.

Table 4.2 Switching states in a Three-phase Three-Level Voltage source inverter

Mode	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Phase – A	0 - $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	0- $[H_{a0}]$	1- $[H_{a1}]$	1- $[H_{a1}]$	1- $[H_{a1}]$	1- $[H_{a1}]$	1- $[H_{a1}]$
Phase – B	0- $[H_{b0}]$	0- $[H_{b0}]$	0- $[H_{b0}]$	1- $[H_{b1}]$	1- $[H_{b1}]$	1- $[H_{b1}]$	2- $[H_{b2}]$	2- $[H_{b2}]$	2- $[H_{b2}]$	0- $[H_{b0}]$	0- $[H_{b0}]$	0- $[H_{b0}]$	1- $[H_{b1}]$	1- $[H_{b1}]$
Phase – C	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$

Mode	15	16	17	18	19	20	21	22	23	24	25	26	27
Phase – A	1- $[H_{a1}]$	1- $[H_{a1}]$	1- $[H_{a1}]$	1- $[H_{a1}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$	2- $[H_{a2}]$
Phase – B	1- $[H_{b1}]$	2- $[H_{b2}]$	2- $[H_{b2}]$	2- $[H_{b2}]$	0- $[H_{b0}]$	0- $[H_{b0}]$	0- $[H_{b0}]$	1- $[H_{b1}]$	1- $[H_{b1}]$	1- $[H_{b1}]$	2- $[H_{b2}]$	2- $[H_{b2}]$	2- $[H_{b2}]$
Phase – C	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$	0- $[H_{c0}]$	1- $[H_{c1}]$	2- $[H_{c2}]$

The next step in the modulation scheme is to find the equivalent voltages generated in each state. The voltages generated are expressed in the stationary reference frame. The qdo voltages of all the switching modes, also given in Table 4.3, are expressed in complex variable form as

$$v_{qds} = \frac{2}{3}\left(v_{an} + av_{bn} + a^2 v_{cn}\right) \tag{4.129}$$

$$V_o = \frac{1}{3}\left(v_{an} + v_{bn} + v_{cn}\right) \tag{4.130}$$

where $a = e^{j\zeta}, \zeta = 120^0$.

The voltage space vectors of a three-phase converter are always located in the plane, and that is how they are represented in Figure 4.8. The space vector is comprised of 24 sectors of which the sector numbered from 1 – 6 are inner hexagon sectors and sector from 7 – 24 are outer hexagon. In general for a N-level converter, the space vector diagram has (N^3 – N) sectors. The number of hexagons increases as the number of levels increase. For a N-level converter, there are (N-1) hexagons.

Table 4.3: The corresponding stationary reference frame qdo voltages of three-phase three-level voltage source inverter.

Mode	1	2	3	4	5	6	7	8	9	10	11	12	13
q-axis voltage V_q	0	$-\frac{V_d}{6}$	$-\frac{V_d}{2\sqrt{3}}$	$-\frac{V_d}{6}$	$-\frac{V_d}{3}$	$-\frac{V_d}{2}$	$-\frac{V_d}{3}$	$-\frac{V_d}{2}$	$-\frac{2V_d}{3}$	$\frac{V_d}{3}$	$\frac{V_d}{6}$	0	$\frac{V_d}{6}$
d-axis voltage V_d	0	$\frac{V_d}{2\sqrt{3}}$	$\frac{V_d}{\sqrt{3}}$	$-\frac{V_d}{2\sqrt{3}}$	0	$\frac{V_d}{2\sqrt{3}}$	$\frac{V_d}{\sqrt{3}}$	$-\frac{V_d}{2\sqrt{3}}$	0	0	$\frac{V_d}{2\sqrt{3}}$	$\frac{V_d}{\sqrt{3}}$	$-\frac{V_d}{2\sqrt{3}}$
Zero sequence voltage V_0	$-\frac{V_d}{2}$	$-\frac{V_d}{3}$	$-\frac{V_d}{6}$	$-\frac{V_d}{3}$	$-\frac{V_d}{6}$	0	$-\frac{V_d}{6}$	0	$\frac{V_d}{6}$	$-\frac{V_d}{3}$	$-\frac{V_d}{6}$	0	$-\frac{V_d}{6}$

Mode	14	15	16	17	18	19	20	21	22	23	24	25	26	27
q-axis voltage V_q	0	$-\frac{V_d}{6}$	0	$-\frac{V_d}{6}$	$-\frac{V_d}{3}$	$\frac{2V_d}{3}$	$\frac{V_d}{2}$	$\frac{V_d}{3}$	$\frac{V_d}{2}$	$\frac{V_d}{3}$	$\frac{V_d}{6}$	$\frac{V_d}{3}$	$\frac{V_d}{6}$	0
d-axis voltage V_d	0	$\frac{V_d}{2\sqrt{3}}$	$-\frac{V_d}{\sqrt{3}}$	$-\frac{V_d}{2\sqrt{3}}$	0	0	$\frac{V_d}{2\sqrt{3}}$	$\frac{V_d}{\sqrt{3}}$	$-\frac{V_d}{2\sqrt{3}}$	0	$\frac{V_d}{2\sqrt{3}}$	$-\frac{V_d}{\sqrt{3}}$	$-\frac{V_d}{2\sqrt{3}}$	0
Zero sequence voltage V_0	0	$\frac{V_d}{6}$	0	$\frac{V_d}{6}$	$\frac{V_d}{3}$	$-\frac{V_d}{6}$	0	$\frac{V_d}{6}$	0	$\frac{V_d}{6}$	$\frac{V_d}{3}$	$\frac{V_d}{6}$	$\frac{V_d}{3}$	$\frac{V_d}{2}$

---- Redundant states [(2,15), (4,17), (5,18), (10,23), (11,24), (13,26)] are the pairs of states that redundant i.e., these each redundant state generates the same magnitude of the voltage but have different value of zero sequence voltage.

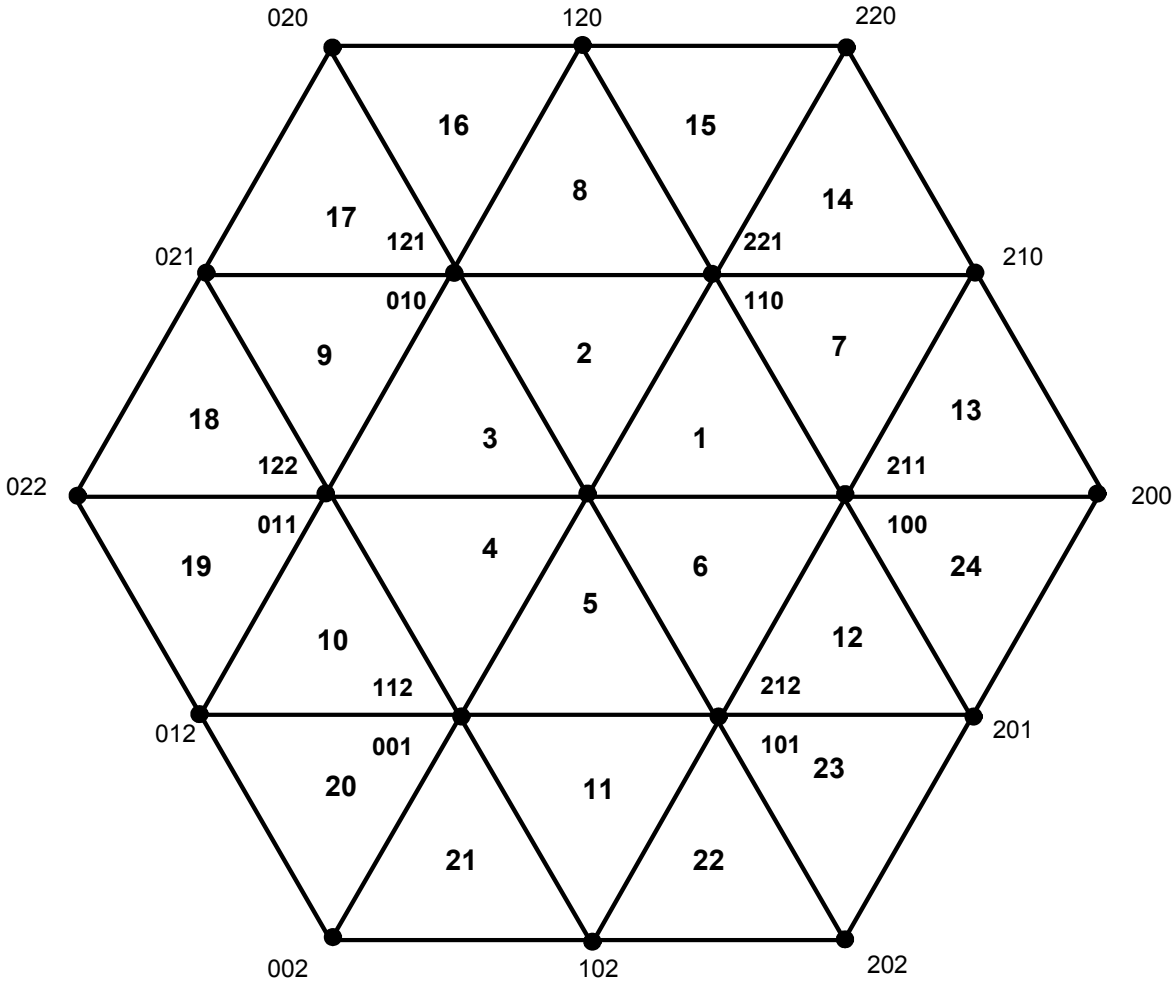


Figure 4.8: Space Vector Diagram of Three-phase three-level voltage source inverter.

As seen from Figure 4.8, the space vector has two hexagons, inner and outer hexagons, formed by 19 vectors. These 19 vectors are combined to form the 24-sector space vector. Naming the switching states with the numbers is much more general (applicable for any level) in which 2, 1, 0, where 2 means that the converter is connected to the positive voltage node, 1 represents the neutral point, and 0 connects to the negative node voltage. Out of the 19 vectors, the vectors corresponding to the inner sectors 1 – 6 are called the small vectors. Also in the inner hexagon there are some redundant vectors at the corners and these redundant vectors synthesize the same reference voltage but they have different zero sequence voltage. Also the currents in these states will be in the opposite directions and hence careful division of time intervals between these states can control the neutral current and the neutral point voltage. The vectors corresponding to the sectors from 7 – 12 are called the medium vectors. During the switching of these vectors the current has only one direction depending on the neutral point voltage. Hence the only vectors, which generate the neutral current, are the medium vectors. Vectors corresponding to the sectors 13 – 24 are known as the large vectors. These vectors do not contribute to the neutral current.

A reference signal V_{qd}^{*} can be defined from the space vector using the vectors. Assuming that T_s is sufficiently small V_{qd}^{*} can be considered approximately constant during this interval, and it is this vector which generates the fundamental behavior of the load.

The continuous space vector modulation technique is based on the fact that every vector V_{qd}^{*} inside the hexagon can be expressed as a weighted average combination of the vectors of the triangle in which the reference vector lies. Therefore, in each cycle

imposing the desired reference vector may be achieved by switching between these states. The nearest three vectors [NTV] concept is being used to divide the time between the states; i.e., the nearest three vectors that are close to the reference vector are determined and the turn on times of the states of the devices are determined depending on the control.

From Figure 4.8 assuming V_{qd}^{*} to be lying in sector k, the vectors are named a, b, c. In order to obtain optimum harmonic performance and minimize the switching losses, the state sequence is arranged such that switching only one inverter leg performs the transition from one state to the next. The central part of the space vector modulation strategy is the computation of switching times of the sectors for each modulation cycle. In the direct digital PWM method, the complex plane stationary reference frame qd output voltage vector of the three-phase voltage source inverter is used to calculate the turn-on times of the switches required to synthesize the reference voltage. In general, the three-phase balanced voltages expressed in the stationary reference frame, situated in the appropriate sector in Figure 4.8 are approximated by the time average over a sampling period of the three vectors. If the normalized times (with respect to modulator sampling time or converter switching period, T_s) of three vectors termed as V_{qda}, V_{qdb}, V_{qdc} corresponds to time signals t_a, t_b, and t_c, respectively, then the q and d components of the reference voltage V_{qd}^{*} are approximated as

$$V_{qd}^{*} = V_{qq} + jV_{dd} = V_{qda}t_a + V_{qdb}t_b + V_{qdc}t_c \tag{4.131}$$

and the devices have to switch according to the following constraint

$$t_a + t_b + t_c = 1. \tag{4.132}$$

Separating the real and imaginary terms in Eqs. (4.131)

$$V_{qq} = \left(V_{qa} - V_{qc}\right)\, t_a + \left(V_{qb} - V_{qc}\right)\, t_b + V_{qc}$$

$$V_{dd} = \left(V_{da} - V_{dc}\right)\, t_a + \left(V_{db} - V_{dc}\right)\, t_b + V_{dc}\,.$$

Expressing the above equations in the matrix form

$$\begin{bmatrix} V_{qq} \\ V_{dd} \end{bmatrix} = \begin{bmatrix} V_{qa} - V_{qc} & V_{qb} - V_{qc} \\ V_{da} - V_{dc} & V_{db} - V_{dc} \end{bmatrix} \begin{bmatrix} t_a \\ t_b \end{bmatrix} + \begin{bmatrix} V_{qc} \\ V_{dc} \end{bmatrix}.$$

By solving the above matrix for t_a, t_b

$$t_a = \frac{V_{qb}V_{dd} - V_{qb}V_{dc} - V_{qc}V_{dd} + V_{qb}V_{qc} - V_{qq}V_{db} + V_{qq}V_{dc}}{\nabla} \tag{4.133}$$

$$t_b = \frac{V_{da}V_{qq} - V_{da}V_{qc} - V_{dc}V_{qq} + V_{dc}V_{qa} - V_{dd}V_{qa} + V_{dd}V_{qc}}{\nabla} \tag{4.134}$$

where

$$\nabla = V_{da}V_{qb} - V_{da}V_{qc} - V_{dc}V_{qb} - V_{db}V_{qa} + V_{db}V_{qc} + V_{dc}V_{qa}\,.$$

Consider for sector 1:

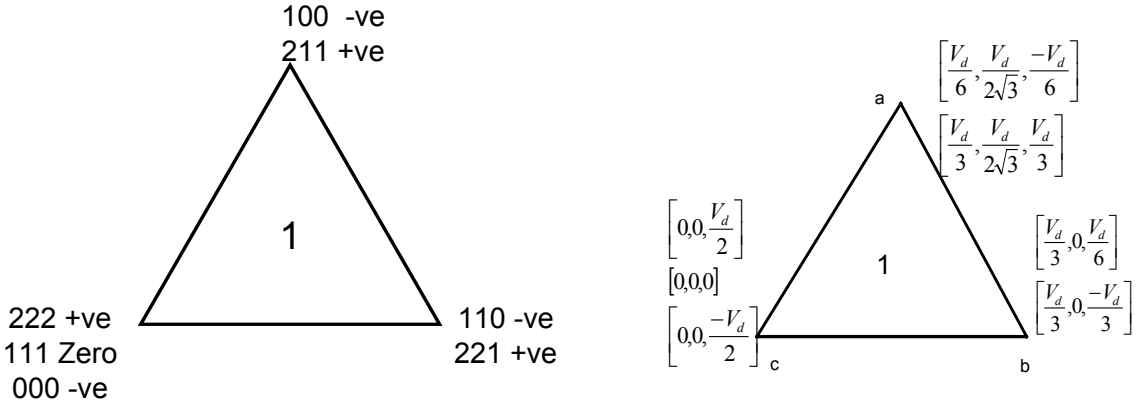


Figure 4.9: Sector 1 of the space vector diagram.

The voltages for the three vectors that correspond to sector 1 are

$$V_{qa} = \frac{V_d}{6}; V_{da} = \frac{V_d}{2\sqrt{3}}$$

$$V_{qb} = \frac{V_d}{3}; V_{da} = 0$$

$$V_{qc} = 0; V_{dc} = 0.$$

Hence by substituting the above known terms in Eqs. (4.133)-(4.134), the turn on times of the devices is obtained as

$$t_a = \frac{0.5}{V_d}[3V_{qq} - \sqrt{3}V_{dd}]$$

$$t_b = \frac{\sqrt{3}V_{dd}}{V_d}.$$

Hence in the similar way in each sector the turns on times of the devices are calculated and are enlisted in Table 4.4. These timings are in terms of the reference qd voltages.

Thus the mentioned procedure is used for microprocessor or DSP-based implementation of the space vector PWM [33-40]. The state diagram corresponding to each sector is drawn and the pattern has to be loaded into the DSP to turn on the devices. Figure 4.9 shows the state diagram for sector 1. In space vector the states have to be sequenced to obtain minimum switching but this sequencing is not necessary in the carrier-based PWM technique. The technique is explained in the following section.

Table 4.4 Device-switching times expressed in terms of qd reference voltage.

Sector	t_a	t_b
1	$\frac{0.5}{V_d}[3V_{qq} - \sqrt{3}V_{dd}]$	$\frac{\sqrt{3}V_{dd}}{V_d}$
2	$\frac{0.5}{V_d}[3V_{qq} + \sqrt{3}V_{dd}]$	$-\frac{0.5}{V_d}[-3V_{qq} + \sqrt{3}V_{dd}]$
3	$-\frac{\sqrt{3}V_{dd}}{V_d}$	$-\frac{0.5}{V_d}[3V_{qq} + \sqrt{3}V_{dd}]$
4	$\frac{0.5}{V_d}[-3V_{qq} + \sqrt{3}V_{dd}]$	$-\frac{\sqrt{3}V_{dd}}{V_d}$
5	$-\frac{0.5}{V_d}[3V_{qq} + \sqrt{3}V_{dd}]$	$-\frac{0.5}{V_d}[3V_{qq} - \sqrt{3}V_{dd}]$
6	$\frac{\sqrt{3}V_{dd}}{V_d}$	$\frac{0.5}{V_d}[3V_{qq} + \sqrt{3}V_{dd}]$
7	$\frac{2\sqrt{3}V_{dd}}{V_d}$	$\frac{3V_{qq} - \sqrt{3}V_{dd}}{V_d} - \frac{2\sqrt{3}V_{dd}}{V_d}$
8	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - V_{dd}]$	$\frac{2}{V_d}[3V_{qq} + \sqrt{3}V_{dd}] - \frac{2\sqrt{3}V_{dd}}{V_d}$
9	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + 3V_{dd}]$	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + V_{dd}]$
10	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - 3V_{dd}]$	$-\frac{2\sqrt{3}V_{dd}}{V_d}$
11	$-\frac{6V_{qq}}{V_d}$	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - V_{dd}]$
12	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + V_{dd}]$	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + 3V_{dd}]$
13	$-\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - 3V_{dd}]$	$\frac{2\sqrt{3}V_{dd}}{V_d}$
14	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - V_{dd}]$	$-\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - 3V_{dd}]$

Table 4.4:Continued

Sector	t_a	t_b
15	$\frac{3V_{qq}}{V_d}$	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - V_{dd}]$
16	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + V_{dd}]$	$-\frac{3V_{qq}}{V_d}$
17	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + V_{dd}]$	$\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + 3V_{dd}]$
18	$\frac{2\sqrt{3}V_{dd}}{V_d}$	$-\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + 3V_{dd}]$
19	$-\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - 3V_{dd}]$	$-\frac{2\sqrt{3}V_{dd}}{V_d}$
20	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - V_{dd}]$	$\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - 3V_{dd}]$
21	$-\frac{3V_{qq}}{V_d}$	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} - V_{dd}]$
22	$-\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + V_{dd}]$	$\frac{3V_{qq}}{V_d}$
23	$-\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + 3V_{dd}]$	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + V_{dd}]$
24	$-\frac{2\sqrt{3}V_{dd}}{V_d}$	$\frac{0.5\times\sqrt{3}}{V_d}[\sqrt{3}V_{qq} + 3V_{dd}]$

State diagram:

Figure 4.10 shows the state diagram corresponding to sector 1. Consider sector 1 A, from Figure 4.8; the available vectors are U_b (100 (-), 211 (+)), U_a (110(-), 221 (+)), U_c

(222(+), 111(0), 000(-)). The variable α is used to divide the time interval t_c between the positive (222) and zero vector (000) or the negative (111) and the zero vector (000). The vectors corresponding to 1A are U_a (221), U_a (211), and U_c(000, 111). The time for which the devices corresponding to sector 1A are turned on is shown in Table 4.5 as the existence functions.

Table 4.5: Existence functions for all the devices corresponding to sector 1.

	H_{a1}	H_{a2}	H_{a3}	H_{b1}	H_{b2}	H_{b3}	H_{c1}	H_{c2}	H_{c3}
1A	0	$t_a+t_b+\beta t_c$	αt_c	βt_c	$\alpha t_c+t_a+t_b$	0	$t_b+\beta t_c$	αt_c+t_a	0
1B	0	$t_b+\beta t_c$	αt_c+t_a	0	$t_a+t_b+\beta t_c$	$\alpha\ t_c$	βt_c	$\alpha t_c+t_a+t_b$	0

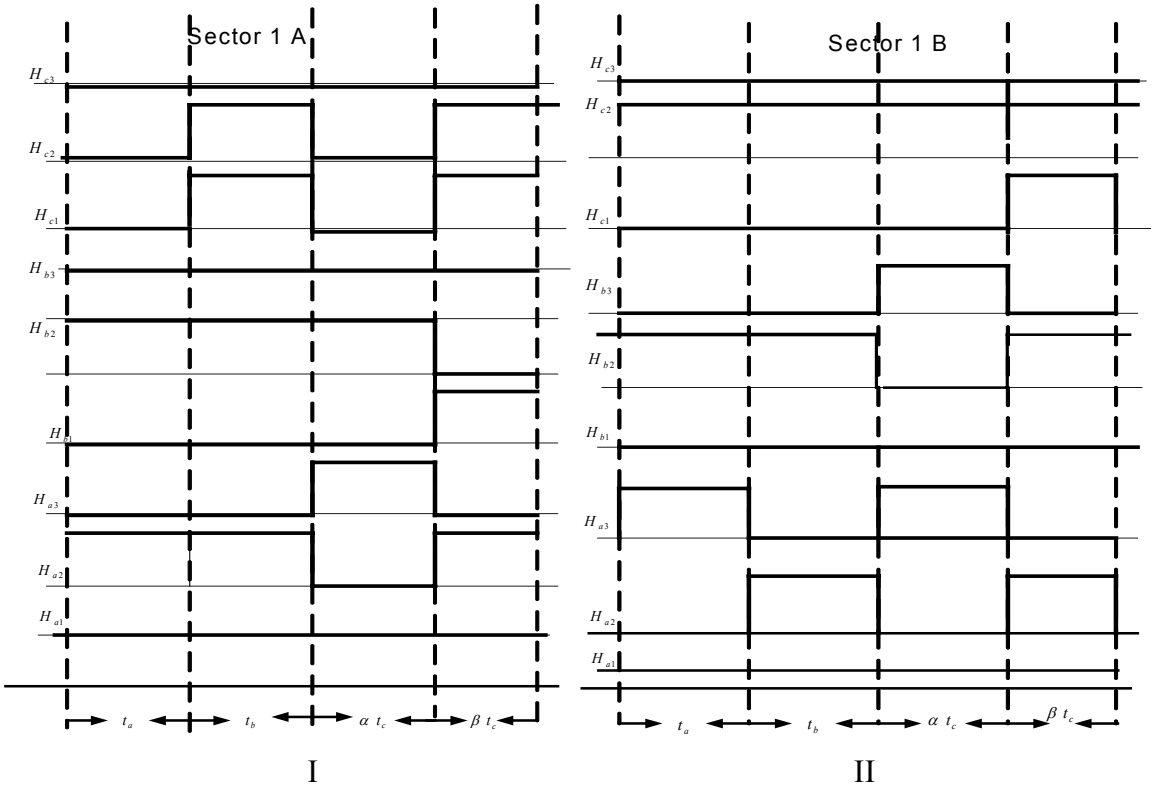


Figure 4.10: State diagram corresponding to (I) sector 1 A, (II) sector 1 B.

4.5.2 Carrier-based Implementation of Space Vector Modulation SVPWM

In the carrier-based implementation of the space vector modulation, the equivalent modulation signals are determined for the timing expression using the space vector principle such that when the modulation signal is compared with the carrier waveform turns on the device for the same amount of time. Hence in a way the sine-triangle and the space vector modulation are exactly equivalent in every way [76-77]. In the carrier- based implementation, the Phase Disposition (PD) technique is used. Figure 4.7 shows the reference and the carrier waveform arrangements required to achieve this form of modulation for three-level inverter. In Figure 4.1 the important criteria to satisfy KVL and KCL is

$$H_{a3} + H_{a2} + H_{a1} = 1$$

$$H_{b3} + H_{b2} + H_{b1} = 1$$

$$H_{c3} + H_{c2} + H_{c1} = 1$$

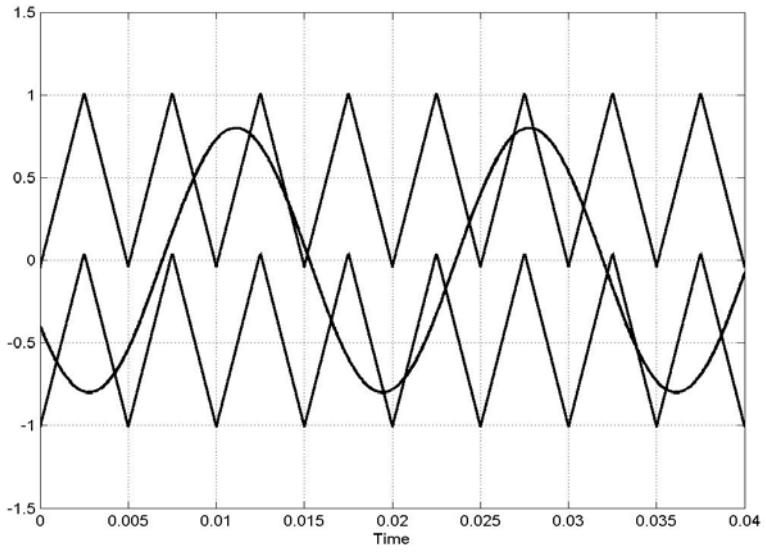


Figure 4.11: Carrier-based PWM using the phase disposition technique.

where H_{ij} are switching functions and are defined as when compared with two triangles equally displaced.

$$V_{abc} > Triangle - 1 \;\; \&$$
$$> Triangle - 2; \;\; H_{i3} = 1; \;\; otherwise \quad H_{i3} = 0$$

$$V_{abc} < Triangle - 1 \;\; \&$$
$$> Triangle - 2; \;\; H_{i2} = 1; \;\; otherwise \quad H_{i2} = 0$$

$$V_{abc} < Triangle - 1 \;\; \&$$
$$< Triangle - 2; \;\; H_{i1} = 1; \;\; otherwise \quad H_{i1} = 0$$

The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage V_{30}, V_{20}, V_{10} is given by Eqs. (4.1 - 4.3). The quantities v_{ao}, v_{bo}, v_{co} are the output voltages of the inverter with respect to the neutral point of the two capacitors. V_{20} is the neutral voltage which is floating between the neutral of the load and the neutral point of the two capacitors. This voltage may assume any value and hence becomes a part of the control.

4.5.3 Determination of the qdo Voltages of the Switching Modes

The stationary reference frame qdo voltages of the switching modes, also given in Table 4.2 are expressed as

$$f_q = \frac{1}{3}\left(2f_a - f_b - f_c\right) \tag{4.135}$$

$$f_d = \frac{1}{\sqrt{3}}(f_b - f_c) \tag{4.136}$$

$$f_o = \frac{1}{3}(f_a + f_b + f_c). \tag{4.137}$$

In the present case f_q , f_d, f_o are v_{ao}, v_{bo}, v_{co}.

For example for the state 1 from Table 4.1, the qdo voltages are determined as follows. Since the converter in state 1 is being connected to the negative voltage for all the three phases, the output voltages are

$$v_{ao} = V_0$$
$$v_{bo} = V_0$$
$$v_{co} = V_0.$$

Hence the qdo voltages are given by

$$V_q = \frac{1}{3}(2V_0 - V_0 - V_0) = 0$$
$$V_d = \frac{1}{\sqrt{3}}(V_0 - V_0) = 0$$
$$V_o = \frac{1}{3}(V_0 + V_0 + V_0) = V_0 = -\frac{V_d}{2}.$$

Under balanced conditions, $V_2 = \frac{V_d}{2}$; $V_1 = -0$; $V_0 = -\frac{V_d}{2}$.

Hence in the similar way, the qd voltages of the other valid states are calculated.

4.5.4 Determination of the Device Switching Times Expressed in Terms of Line-Line Reference Voltage

The device timings that are calculated in section 4.2 are in terms of the qd voltages. The next step in the carrier-based PWM implementation is expressing the

timing expression in terms of the reference line-line voltages. Hence the timing expressions, which are in terms of the qd voltages, are transformed to abc reference frame.

The stationary reference frame inverse transformation is given as

$$f_a = f_q + f_o$$

$$f_b = -\frac{f_q}{2} - \frac{\sqrt{3}}{2} f_d + f_o$$

$$f_c = -\frac{f_q}{2} + \frac{\sqrt{3}}{2} f_d + f_o .$$

Now

$$f_a - f_b = f_{ab} = f_q + f_o + \frac{f_q}{2} + \frac{\sqrt{3}}{2} f_d - f_o = \frac{0.5}{V_d}\left(3 f_q + \sqrt{3} f_d\right) \tag{4.138}$$

$$f_a - f_c = f_{ac} = f_q + f_o + \frac{f_q}{2} - \frac{\sqrt{3}}{2} f_d - f_o = \frac{0.5}{V_d}\left(f_q - \sqrt{3} f_d\right) \tag{4.139}$$

$$f_b - f_c = f_{bc} = -\frac{f_q}{2} - \frac{\sqrt{3}}{2} f_d + f_o + \frac{f_q}{2} - \frac{\sqrt{3}}{2} f_d - f_o = -\sqrt{3} V_d . \tag{4.140}$$

Consider sector 6:

The devices in qd reference voltage are obtained in the above section as

$$t_a = \frac{0.5}{V_d}[3V_{qq} - \sqrt{3}V_{dd}] = V_{ac} \quad \text{- From Eq. (4.133)}$$

$$t_b = \frac{\sqrt{3}V_{dd}}{V_d} = V_{cb} . \quad \text{- From Eq. (4.134)}$$

Hence using the above transformation, the timing expressions can be expressed in terms of the line-line voltages. The timings in terms of the line-line voltages are tabulated in Table 4.6.

Table 4.6 Device-switching times expressed in terms of reference line-line voltage.

Sector	1	2	3	4	5	6	7	8	9
t_a	$\frac{v_{ac}}{V_d}$	$\frac{v_{ab}}{V_d}$	$\frac{v_{cb}}{V_d}$	$\frac{v_{ca}}{V_d}$	$\frac{v_{ba}}{V_d}$	$\frac{v_{bc}}{V_d}$	$\frac{2v_{cb}}{V_d}$	$\frac{4v_{ab}-2v_{cb}}{V_d}$	$\frac{2}{V_d}[v_{cb}+v_{ab}$
t_b	$\frac{v_{cb}}{V_d}$	$\frac{v_{ca}}{V_d}$	$\frac{v_{ba}}{V_d}$	$\frac{v_{bc}}{V_d}$	$\frac{v_{ac}}{V_d}$	$\frac{v_{ab}}{V_d}$	$\frac{2}{V_d}[v_{ac}-v_{cb}$	$\frac{2v_{ca}}{V_d}$	$\frac{2v_{ba}}{V_d}$

Sector	13	14	15	16	17	18	19
t_a	$\frac{v_{bc}+v_{ac}}{V_d}$	$\frac{2v_{ac}}{V_d}$	$\frac{2v_{ab}-v_{cb}}{V_d}$	$\frac{2v_{ab}}{V_d}$	$\frac{v_{ab}+v_{cb}}{V_d}$	$\frac{-[v_{ab}+v_{cb}]}{V_d}$	$\frac{-[v_{ac}+v_{bc}]}{V_d}$
t_b	$\frac{2v_{cb}}{V_d}$	$\frac{-[v_{ac}-v_{cb}]}{V_d}$	$\frac{2v_{ca}}{V_d}$	$\frac{2v_{ba}+v_{cb}}{V_d}$	$\frac{2v_{ba}}{V_d}$	$\frac{2v_{cb}}{V_d}$	$\frac{2v_{bc}}{V_d}$

Sector	20	21	22	23	24
t_a	$\frac{2v_{ca}}{V_d}$	$\frac{2v_{ca}+v_{bc}}{V_d}$	$\frac{2v_{ba}}{V_d}$	$\frac{-[v_{ab}+v_{cb}]}{V_d}$	$\frac{2v_{bc}}{V_d}$
t_b	$\frac{v_{ac}+v_{bc}}{V_d}$	$\frac{2v_{ac}}{V_d}$	$\frac{2v_{ab}+v_{bc}}{V_d}$	$\frac{2v_{ab}}{V_d}$	$\frac{v_{ab}+v_{cb}}{V_d}$

Table 4.6 Device-switching times expressed in terms of reference line-line voltage.

Sector	1	2	3	4	5	6	7	8	
t_a	$\frac{v_{ac}}{V_d}$	$\frac{v_{ab}}{V_d}$	$\frac{v_{cb}}{V_d}$	$\frac{v_{ca}}{V_d}$	$\frac{v_{ba}}{V_d}$	$\frac{v_{bc}}{V_d}$	$\frac{2v_{cb}}{V_d}$	$\frac{4v_{ab}-2v_{cb}}{V_d}$	
t_b	$\frac{v_{cb}}{V_d}$	$\frac{v_{ca}}{V_d}$	$\frac{v_{ba}}{V_d}$	$\frac{v_{bc}}{V_d}$	$\frac{v_{ac}}{V_d}$	$\frac{v_{ab}}{V_d}$	$\frac{2}{V_d}[v_{ac}-v_{cb}$	$\frac{2v_{ca}}{V_d}$	

Sector	13	14	15	16	17	18	19
t_a	$\frac{v_{bc}+v_{ac}}{V_d}$	$\frac{2v_{ac}}{V_d}$	$\frac{2v_{ab}-v_{cb}}{V_d}$	$\frac{2v_{ab}}{V_d}$	$\frac{v_{ab}+v_{cb}}{V_d}$	$\frac{-[v_{ab}+v_{cb}]}{V_d}$	$\frac{-[v_{ac}$
t_b	$\frac{2v_{cb}}{V_d}$	$\frac{-[v_{ac}-v_{cb}]}{V_d}$	$\frac{2v_{ca}}{V_d}$	$\frac{2v_{ba}+v_{cb}}{V_d}$	$\frac{2v_{ba}}{V_d}$	$\frac{2v_{cb}}{V_d}$	$\frac{2}{V}$

Sector	20	21	22	23	24
t_a	$\frac{2v_{ca}}{V_d}$	$\frac{2v_{ca}+v_{bc}}{V_d}$	$\frac{2v_{ba}}{V_d}$	$\frac{-[v_{ab}+v_{cb}]}{V_d}$	$\frac{2v_{b}}{V_d}$
t_b	$\frac{v_{ac}+v_{bc}}{V_d}$	$\frac{2v_{ac}}{V_d}$	$\frac{2v_{ab}+v_{bc}}{V_d}$	$\frac{2v_{ab}}{V_d}$	$\frac{v_{ab}+}{V_d}$