CHAPTER 8

THREE-PHASE TWO-LEG THREE-LEVEL NEUTRAL POINT CLAMPED RECTIFIER

8.1 Introduction

Three-level neutral point clamped converters were proposed in [4-6] to draw the sinusoidal line currents in phase with the supply voltage. The input power factor is close to unity. However, 12 power switches and six clamping diodes are used in the circuit configuration. Low cost ac drives with four power switches were proposed [73-76] to achieve power factor correction and to perform two-level PWM operation. However this topology is not suitable for medium voltage applications. Hence a topology with less number of devices is being proposed. The proposed converter with less number of devices can be used in the high power or medium voltage applications such as shunt active filters, series active filters [69], hybrid active power filter, ac voltage regulator, and ac motor drives. The PWM switching schemes play the most important role in voltage source inverters or converters for high performance ac motor drives and reactive power compensation systems.

Objective of the Control Scheme:

- To obtain a constant DC bus voltage.
- To balance the capacitor voltages.
- To draw sinusoidal currents with unity power factor.
- Bidirectional power flow.

8.2 Circuit Configuration

The schematic of the adopted three-level two-leg rectifier is shown in Figure 8.1. The phase "c" on the input side is directly connected to the midpoint of the split capacitors. There are four power switches for each phase with a voltage rating of V_{dc} / 2 and four clamping diodes to clamp the dc-voltage with a voltage rating of V_{dc} / 2. The converter consists of a boost inductor L_s on the ac side to filter out the input harmonic current and achieve sinusoidal current waveforms. R_s is the series equivalent resistor. The dc side of the rectifier consists of a split capacitor C_1 and C_2. The two capacitors have the same capacitance i.e., $C_1 = C_2 = C$. A load resistor R_L is connected across the split capacitor. The input side of the rectifier consists of a three-phase balanced voltage sources. The input phase currents are represented using i_a, i_b, i_c and the node currents are represented by I_3, I_2, I_1.

Table 8.1: Description of the circuit components.

Component	Description
R_s	Input side series resistance
L_s	Input side boost inductor
C_1, C_2	Dc split capacitors
R_L	Load resistance
v_a, v_b, v_c	Three-phase ac supply
i_a, i_b, i_c	Three-phase input currents
I_3, I_2, I_1	Output node currents

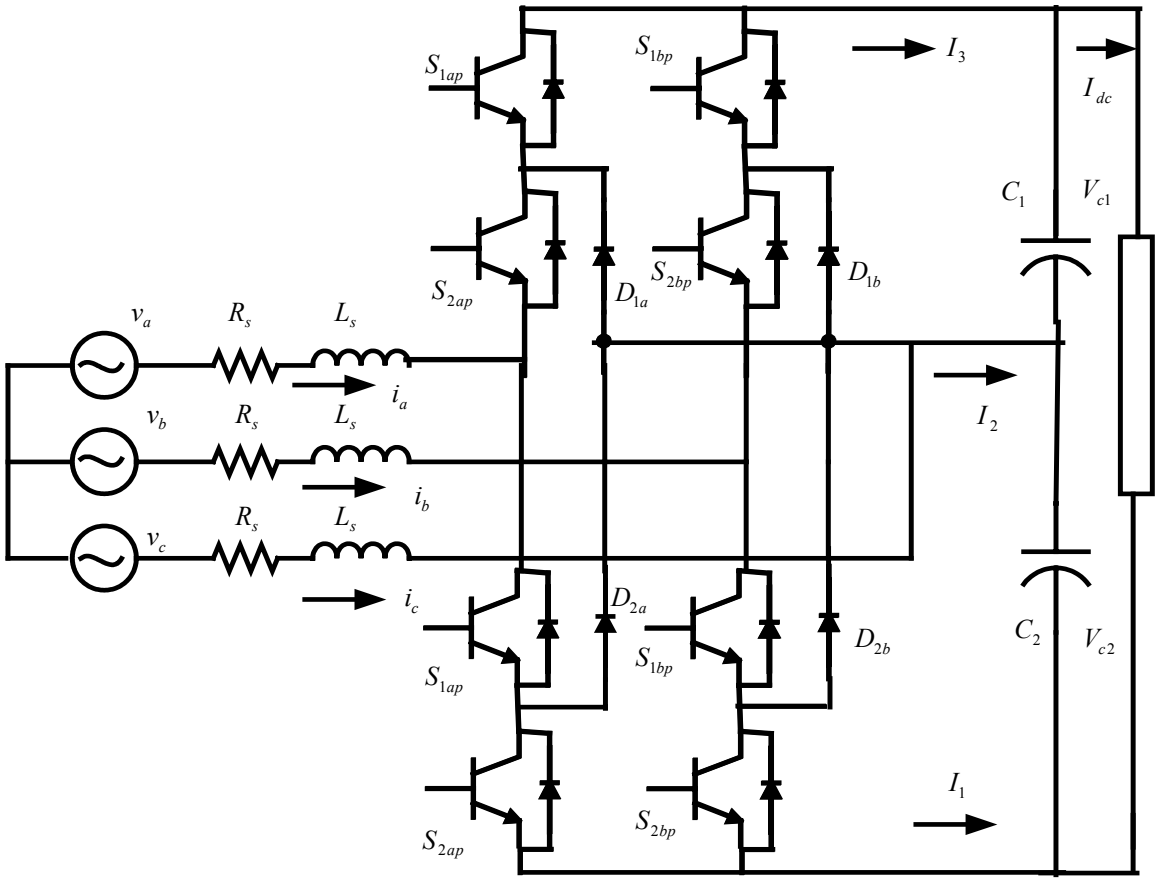

Figure 8.1: Schematic of Three-phase three-level two-leg rectifier.

8.3 Modes of Operations of Two-Leg Three-Level Rectifier

In the case of the two-leg three-phase rectifier there are a total of nine possible states, which are tabulated in Table 8.2. As seen from Table 8.1 it is clear that there three valid states for each leg.

Table 8.2 Possible modes of operation of two-leg three-level rectifier

Mode of Operation	Phase – A	Phase – B
1	2 -$[H_{a3}]$	2-$[H_{b3}]$
2	2-$[H_{a3}]$	1-$[H_{b1}]$
3	2-$[H_{a3}]$	0-$[H_{b0}]$
4	1-$[H_{a1}]$	2-$[H_{b2}]$
5	1-$[H_{a1}]$	1-$[H_{b1}]$
6	1-$[H_{a1}]$	0-$[H_{b0}]$
7	0-$[H_{a0}]$	2-$[H_{b2}]$
8	0-$[H_{a0}]$	1-$[H_{b1}]$
9	0-$[H_{a0}]$	0-$[H_{b0}]$

Mode 1:

In this mode of operation the top two switches in both the legs are turned on; i.e., S_{1ap}, S_{2ap} of phase-A and S_{1bp}, S_{2bp} of phase-B and current i_a and i_b are decreased because $\frac{V_{dc}}{2} > v_{ab},\ v_{bc},\ v_{ca}$. From Figure 8.2 the node current I_3 charges the upper capacitor. The current I_c is increased because of the condition $i_a + i_b + i_c = 0$. The output line-line voltages in this mode are $v_{ac} = \frac{V_{dc}}{2},\ v_{bc} = \frac{V_{dc}}{2},\ v_{ab} = 0$.

The capacitor equation in this mode will be

$$C_1 p V_{c1} = -I_{dc} + H_{a3} i_a + H_{b3} i_b . \tag{8.1}$$

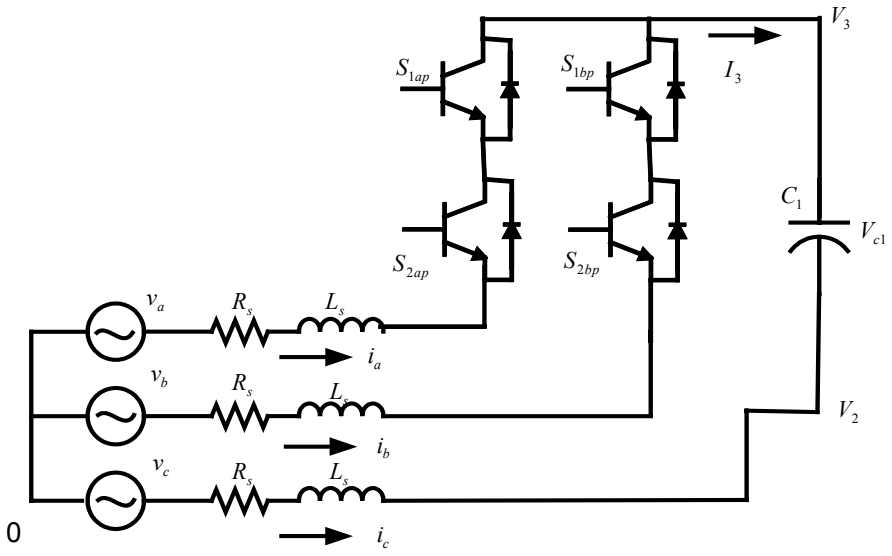

Figure 8.2: Mode 1 operation of three-phase three-level two-leg rectifier.

Mode 2:

In mode 2 of operation the top two switches in leg A and the middle two devices of leg B are turned on, i.e., S_{1ap}, S_{2ap} of phase-A and S_{2bp}, S_{1bn} of phase-B to decrease the inverter current i_a. From Figure 8.3 the node current I_3 charges the upper capacitor. The current i_c is increased because of the condition $i_a + i_b + i_c = 0$.

The capacitor equation in this mode will be

$$C_1 p V_{c1} = -I_{dc} + H_{a3} i_a . \tag{8.2}$$

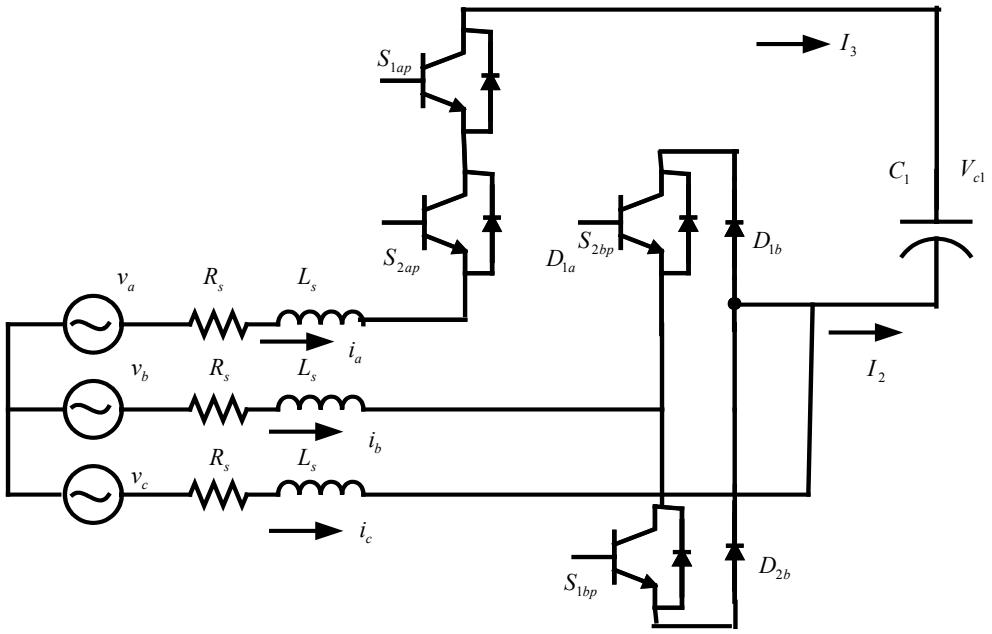

Figure 8.3: Mode 2 operation of three-phase three-level two-leg rectifier.

Mode 3:

The top two switches in the leg A and bottom two switches in the leg B are turned on in this mode; i.e., S_{1ap}, S_{2ap} of phase-A and S_{2bn}, S_{1bn} of phase-B to decrease the inverter current i_a and to increase current i_b. From Figure 8.4 the node currents charge the upper and lower capacitor.

The capacitor equation in this mode will be

$$C_1 pV_{c1} = -I_{dc} + H_{a3} i_a \tag{8.3}$$

$$C_2 pV_{c2} = -\left[I_{dc} + H_{a1} i_b\right]. \tag{8.4}$$

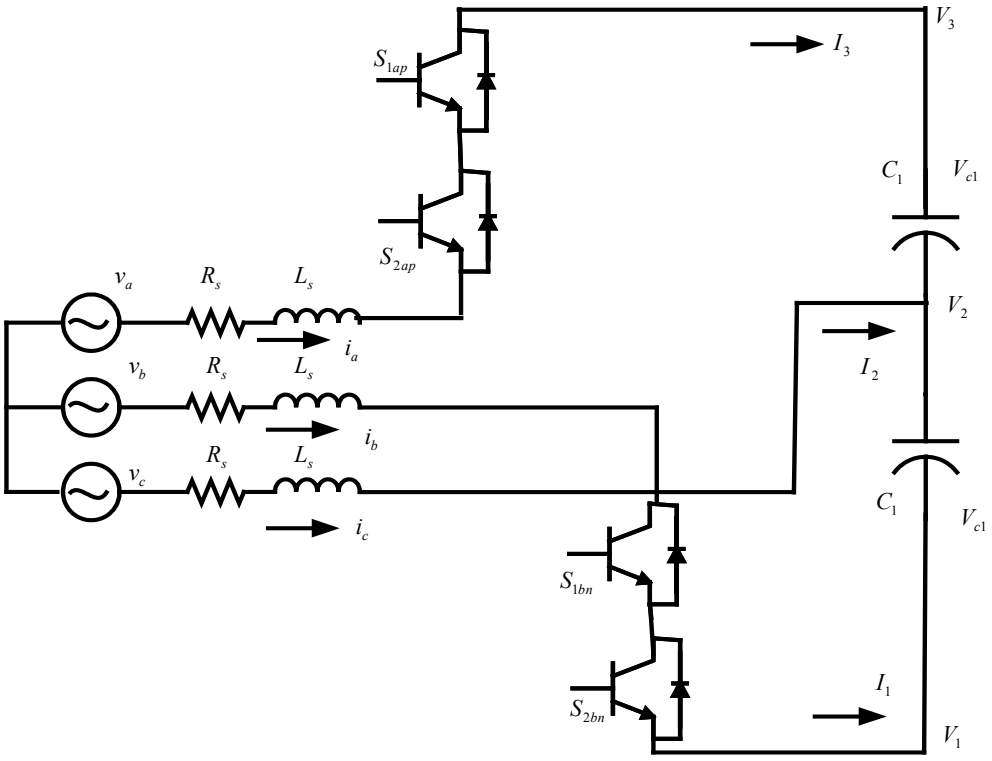

Figure 8.4: Mode 3 operation of three-phase three-level two-leg rectifier.

Mode 4:

In mode 4 operation the top two switches in leg B and the middle two devices of leg A are turned on; i.e., S_{1an}, S_{2an} of phase-A and S_{2bp}, S_{1bp} of phase-B. The line current i_a increases or decreases depending on the sign of the line –line voltage V_{ac} whether it is positive or negative, respectively. The line current i_b also decreases and charges the capacitor C_1. From Figure 8.5, the node current I_3 charges the upper capacitor. The capacitor equation in this mode will be

$$C_1 p V_{c1} = -I_{dc} + H_{b3} i_b . \tag{8.5}$$

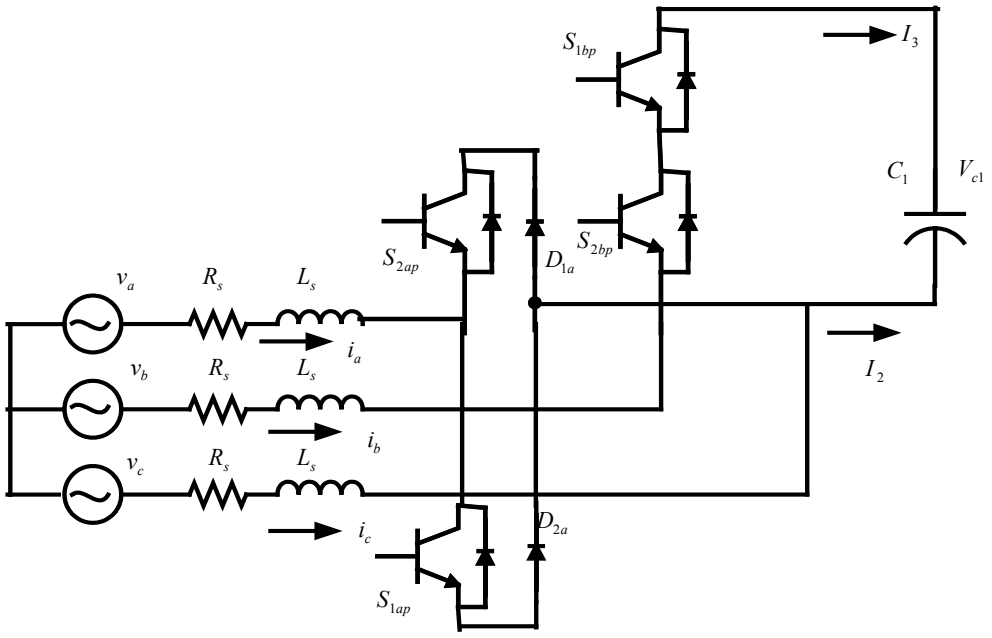

Figure 8.5: Mode 4 operation of three-phase three-level two-leg rectifier.

Mode 5:

In the operation of this mode, two middle switches in leg A and B are turned on; i.e., S_{1an}, S_{2ap} of phase-A and S_{2bp}, S_{1bn} of phase-B. This mode of operation is called as null mode. From Figure 8.6 it is clear that the power devices are not connected to the capacitors and hence neither of the capacitors gets charged. The line current i_a increases or decreases depending on the sign of the line –line voltage v_{ac} whether it is positive or negative, respectively.

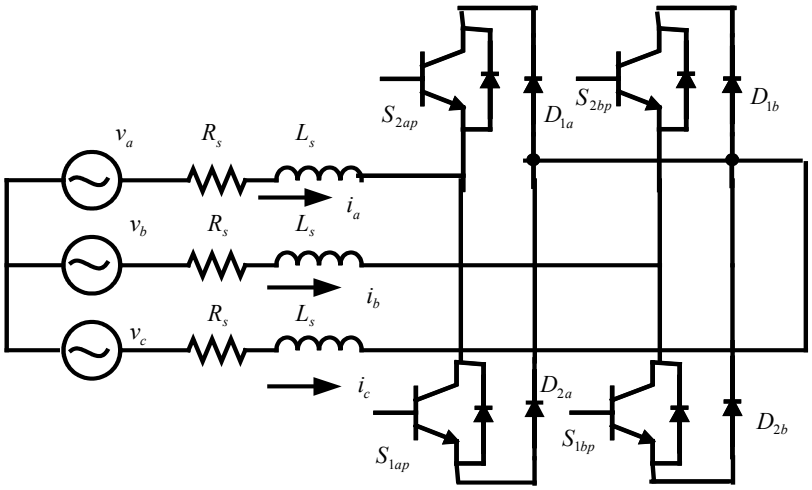

Figure 8.6: Mode 5 operation of three-phase three-level two-leg rectifier.

Mode 6:

In this mode of operation the top two switches in leg A and the middle two devices of leg B are turned on; i.e., S_{1ap}, S_{2ap} of phase-A and S_{2bp}, S_{1bn} of phase-B. The line current i_a increases or decreases depending on the sign of the line –line voltage of v_{ac} whether it is positive or negative, respectively. The line current i_b increases and charges the capacitor C_2. From Figure 8.7 the node current charges the lower capacitor I_1. The capacitor equation in this mode will be

$$C_2 p V_{c2} = -\left[I_{dc} + H_{b1} i_b\right]. \tag{8.6}$$

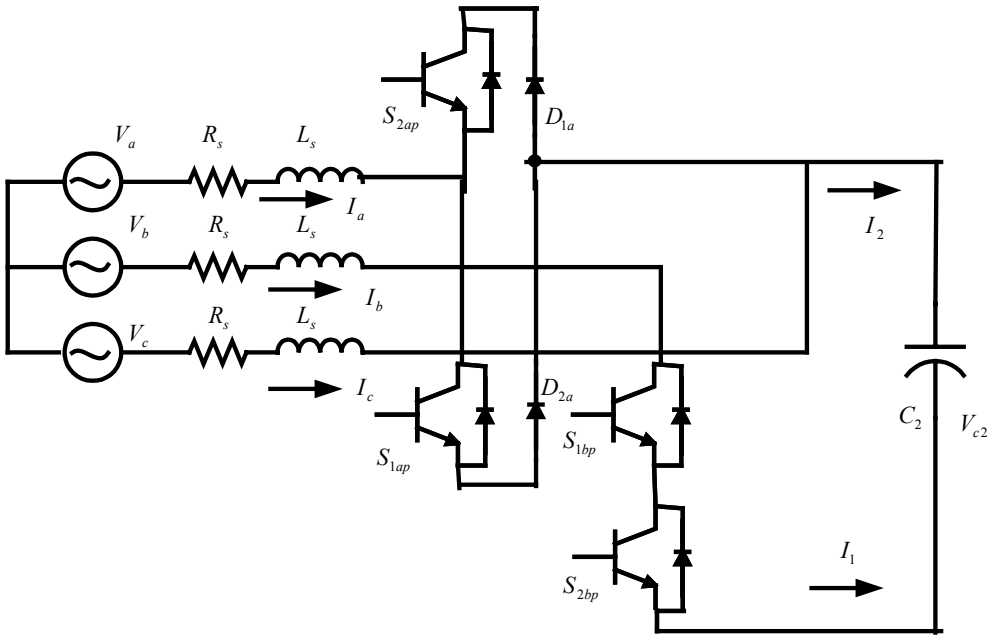

Figure 8.7: Mode 6 operation of three-phase three-level two-leg rectifier.

Mode 7:

In mode 7 the top two switches in leg B and the middle two devices of leg A are turned on; i.e., S_{1an}, S_{2an} of phase-A and S_{2bp}, S_{1bp} of phase-B to increase the line current i_a. From Figure 8.8 the line current i_b decreases and charges both the capacitor C_1 and C_2. The capacitor equation in this mode will be

$$C_1 pV_{c1} = -I_{dc} + H_{b3} i_b \tag{8.8}$$

$$C_2 pV_{c2} = -\left[I_{dc} + H_{a1} i_a\right]. \tag{8.9}$$

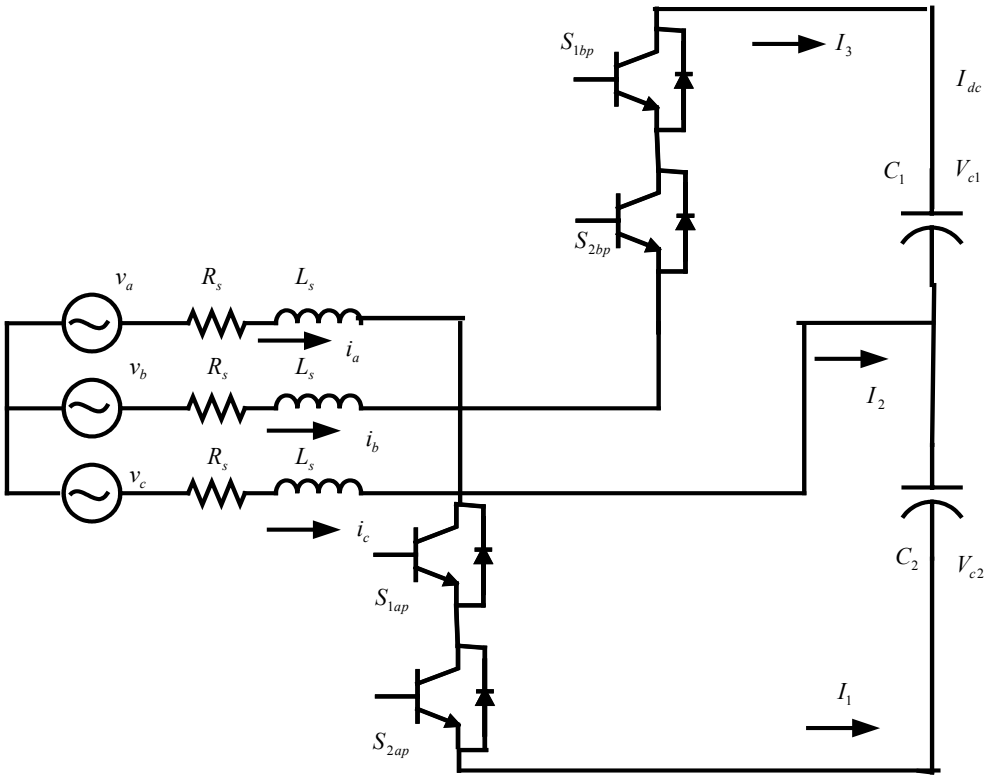

Figure 8.8: Mode 7 operation of three-phase three-level two-leg rectifier.

Mode 8:

In mode 8 of operation the top two switches in leg B and the bottom two devices of leg A are turned on; i.e., S_{1an}, S_{2an} of phase-A and S_{2bp}, S_{1bn} of phase-B to increase the line current i_a. Only capacitor C_2 is charged. The capacitor equation in this mode will be

$$C_2 p V_{c2} = -\left[I_{dc} + H_{a1} i_a\right]. \tag{8.10}$$

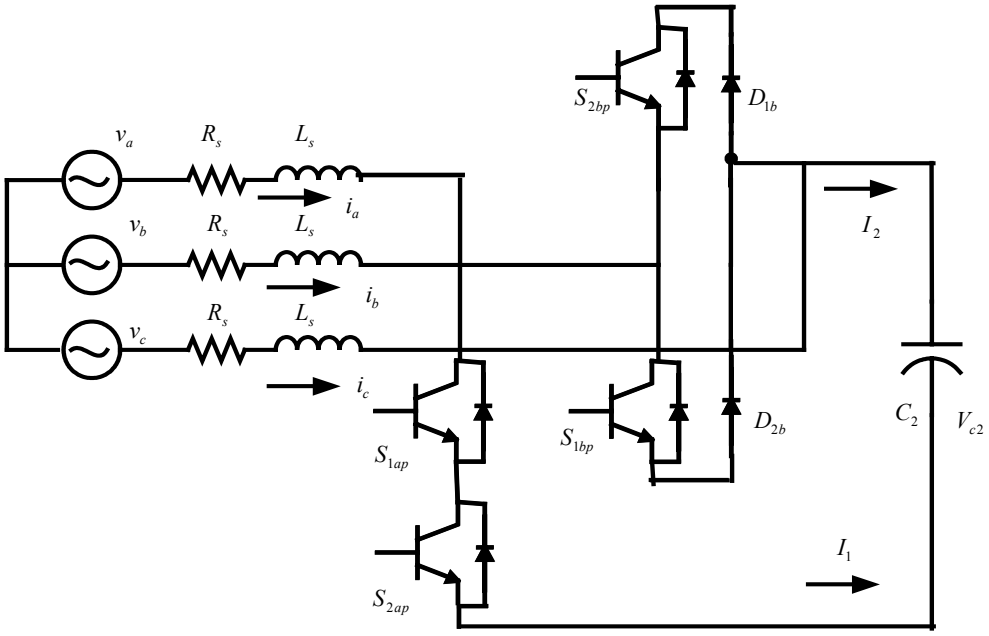

Figure 8.9: Mode 8 operation of three-phase three-level two-leg rectifier.

Mode 9:

In the operation of mode 9 the bottom two switches in leg A and B are turned on; i.e., S_{1an}, S_{2an} of phase-A and S_{2bn}, S_{1bn} of phase-B to increase the line current i_a and i_b. Only the bottom capacitor C_2 is charged. The capacitor equation in this mode will be

$$C_2 p V_{c2} = -\left[I_{dc} + H_{a1} i_a + H_{b1} i_b\right]. \tag{8.11}$$

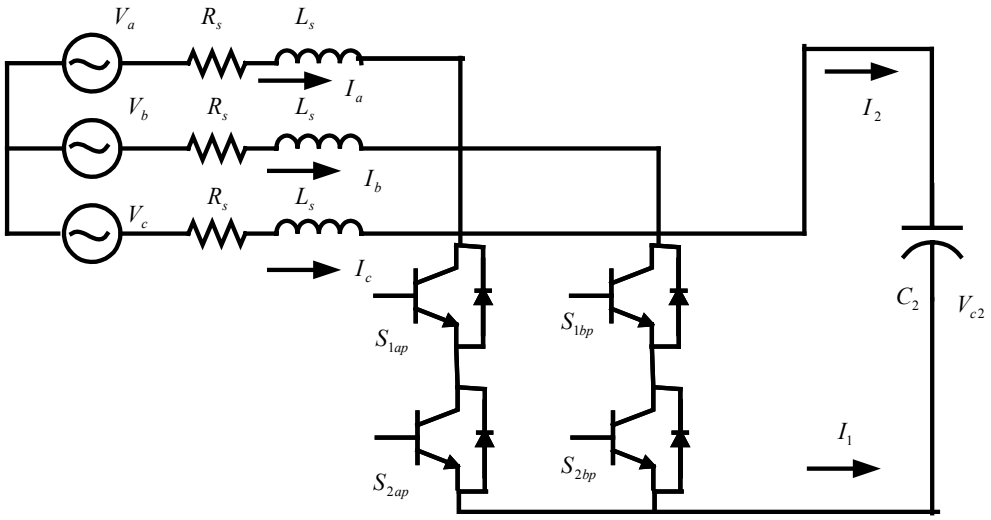

Figure 8.10: Mode 9 operation of three-phase three-level two-leg rectifier.

8.4 Mathematical Model of the Circuit

Applying the Kirchoff's Voltage Law for the input side, we can write the supply voltage as the sum of the voltage drop across the input side impedance and

$$v_a = i_a R_s + L_s p i_a + v_{ao} \tag{8.12}$$

$$v_b = i_b R_s + L_s p i_b + v_{bo} \tag{8.13}$$

$$v_c = i_c R_s + L_s p i_c + v_{co}\,. \tag{8.14}$$

The node voltage V_{30} appears at point 'a' when the upper two switching combination occurs, i.e., when S_{1ap}, S_{2ap} are on. Hence the effective voltage that appears at point 'a' in a cycle is $H_{a3}V_{30}$. Similarly the other two node voltages appear when the other switching combination occurs, i.e., H_{a2} and H_{a1}. Hence the voltage v_{ao} is given by the sum of the three effective voltages

$$v_{ao} = H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10} \tag{8.15}$$

$$v_{bo} = H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10} \tag{8.16}$$

$$v_{co} = V_{20}\,. \tag{8.17}$$

From the switching constraints, in order to avoid the shorting of a leg, the following conditions have to be followed.

$$H_{a3} + H_{a2} + H_{a1} = 1 \tag{8.18}$$

$$H_{b3} + H_{b2} + H_{b1} = 1 \tag{8.19}$$

Consider phase A.

$$H_{a3} + H_{a2} + H_{a1} = 1$$

$$\Rightarrow H_{a2} = 1 - H_{a3} - H_{a1}$$

By substituting the above in output voltage Eq. (8.15)

$$v_{ao} = H_{a3}V_{30} + (1 - H_{a3} - H_{a1})V_{20} + H_{a1}V_{10}$$

$$= H_{a3}(V_{30} - V_{20}) + H_{a1}(V_{10} - V_{20}) + V_{20}$$

$$= H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20}\,.$$

V_{20} is the voltage between the neutral of the supply to the common point of the two capacitors.

Similarly for the other two phases and

$$v_{ao} = H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20} \tag{8.20}$$

$$v_{bo} = H_{b3}V_{c1} - H_{b1}V_{c2} + V_{20} \tag{8.21}$$

$$v_{co} = V_{20}\,. \tag{8.22}$$

By substituting the expression in Eqs. (8.20-8.22) into Eqs. (8.12-8.14)

$$v_a = i_a R_s + L_s p i_a + H_{a3} V_{c1} - H_{a1} V_{c2} + V_{20} \tag{8.23}$$

$$v_b = i_b R_s + L_s p i_b + H_{b3} V_{c1} - H_{b1} V_{c2} + V_{20} \tag{8.24}$$

$$v_c = i_c R_s + L_s p i_c + V_{20}. \tag{8.25}$$

Under balanced condition, from the above

$$V_{20} = -\frac{1}{3}\left[V_{c1}\left(H_{a3} + H_{b3}\right) + V_{c2}\left(H_{a1} + H_{b1}\right)\right]. \tag{8.26}$$

As explained in Chapter 4, the switching function of the devices is

$$H_{a3} = \left(\frac{2v_{a0}}{V_d} + 1\right)\frac{1}{3} \quad , \; H_{a2} = \frac{1}{3}, \; H_{a1} = \left(-\frac{2v_{a0}}{V_d} + 1\right)\frac{1}{3}. \tag{8.27}$$

The switching pulses can be represented as sum of dc component and cosine or sine varying term as

$$H_{a3} = \left(M_{a3} + 1\right)\frac{1}{3}. \tag{8.28}$$

where M_{a3} is called the modulation signal.

By equating the switching functions and Eq. (8.28),

$$\left(\frac{2v_{a0}}{V_d} + 1\right)\frac{1}{3} = \left(M_a + 1\right)\frac{1}{3}.$$

Hence the modulation signal for the top devices is

$$M_{a3} = \frac{2v_{a0}}{V_d}. \tag{8.29}$$

Similarly for the other devices, the modulation signal is obtained as

$$M_{a2} = 0 \text{ and } M_{a1} = -\frac{2v_{a0}}{V_d}. \tag{8.30}$$

From Eqs. (8.29) and (8.30)

$$M_{a3} = -M_{a1} = H_a \tag{8.31}$$

where H_a is the modulation signal.

Substituting the above conditions in Eqs. (8.23 – 8.25)

$$v_a = i_a R_s + L_s p i_a + H_a \left(V_{c1} + V_{c2}\right) + V_{20} \tag{8.32}$$

$$v_b = i_b R_s + L_s p i_b + H_b \left(V_{c1} + V_{c2}\right) + V_{20} \tag{8.33}$$

$$v_c = i_c R_s + L_s p i_c + V_{20}. \tag{8.34}$$

The node currents are given by

$$I_3 = H_{a3} i_a + H_{b3} i_b \tag{8.35}$$

$$I_2 = H_{a2} i_a + H_{b2} i_b + H_{c2} i_c \tag{8.36}$$

$$I_1 = H_{a1} i_a + H_{b1} i_b . \tag{8.37}$$

Applying Kirchoff's Current Law (KCL) at node 3, i.e., the current flowing through capacitor C_1 is equal to the difference of the node current I_3 and the load current I_{dc} and the current flowing through the capacitor C_2 is given by the KCL equation at node 1.

$$CpV_{c1} = -I_{dc} + H_{a3} i_a + H_{b3} i_b \tag{8.38}$$

$$CpV_{c2} = -\left[I_{dc} + H_{a1} i_a + H_{b1} i_b\right] \tag{8.39}$$

Substituting the condition in Eq. (8.31) in Eq. (8.33) and (8.34), gives

$$CpV_{c1} = -I_{dc} + H_a i_a + H_b i_b \tag{8.40}$$

$$CpV_{c2} = -\left[I_{dc} - H_a i_a - H_b i_b\right]. \tag{8.41}$$

8.5 qdo Modeling of the Converter

Writing Eqs. (8.23-8.25) in the matrix form

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L_s & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & L_s \end{bmatrix} \begin{bmatrix} pi_a \\ pi_b \\ pi_c \end{bmatrix} + \begin{bmatrix} H_{a3} \\ H_{b3} \\ 0 \end{bmatrix} V_{c1} - \begin{bmatrix} H_{a1} \\ H_{b1} \\ 0 \end{bmatrix} V_{c2} + V_{20}.$$

Transforming the above equation to synchronous reference frame using the transformation matrix $T(\theta)$, where

$$T(\theta) = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta-\beta) & \cos(\theta+\beta) \\ \sin(\theta) & \sin(\theta-\beta) & \sin(\theta+\beta) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \beta = \frac{2\pi}{3}$$

$\theta = \int \omega_e dt + \theta_0$; θ_0 - Initial reference angle.

qd equations are obtained as

$$V_q^{\ e} = R_s I_q^{\ e} + L_s p I_q^{\ e} + \omega_e L_s I_d^{\ e} + V_{c1} H_{q3} - V_{c2} H_{q1} \tag{8.42}$$

$$V_d^{\ e} = R_s I_d^{\ e} + L_s p I_d^{\ e} - \omega_e L_s I_q^{\ e} + V_{c1} H_{d3} - V_{c2} H_{d1} \tag{8.43}$$

$$V_0^{\ e} = R_s I_0^{\ e} + L_s p I_0^{\ e} + V_{c1} H_{03} - V_{c2} H_{01} \tag{8.44}$$

$$C_1 p V_{c1} = -I_{dc} + \frac{3}{2}\left[H_{q3} I_q^{\ e} + H_{d3} I_d^{\ e} + H_{03} I_0^{\ e}\right] \tag{8.45}$$

$$C_2 p V_{c2} = -\left[I_{dc} + \frac{3}{2}\left[H_{q1} I_q^{\ e} + H_{d1} I_d^{\ e} + H_{01} I_0^{\ e}\right]\right] \tag{8.46}$$

where

$$H_{q3} = \frac{2}{3}\left[H_{a3}\cos(\theta) + H_{b3}\cos(\theta-\beta)\right]$$

$$H_{d3} = \frac{2}{3}\left[H_{a3}\sin(\theta) + H_{b3}\sin(\theta-\beta)\right]$$

$$H_{03} = \frac{1}{3}\left[H_{a3} + H_{b3}\right].$$

Similarly,

$$H_{q1} = \frac{2}{3}\left[H_{a1}\cos(\theta) + H_{b1}\cos(\theta - \beta) + H_{c1}\cos(\theta + \beta)\right]$$

$$H_{d1} = \frac{2}{3}\left[H_{a1}\sin(\theta) + H_{b1}\sin(\theta - \beta) + H_{c1}\sin(\theta + \beta)\right]$$

$$H_{01} = \frac{1}{3}\left[H_{a1} + H_{b1}\right].$$

Assuming

$$H_{q3} = \alpha H_q ;\ H_{d3} = \alpha H_d$$

$$H_{q1} = -\beta H_q ;\ H_{d1} = -\beta H_d .$$

By substituting the above expressions in Eqs. (8.42 - 8.46)

$$V_q{}^e = R_s I_q{}^e + L_s p I_q{}^e + \omega_e L_s I_d{}^e + \left(\alpha V_{c1} + \beta V_{c2}\right)H_q \tag{8.47}$$

$$V_d{}^e = R_s I_d{}^e + L_s p I_d{}^e - \omega_e L_s I_q{}^e + \left(\alpha V_{c1} + \beta V_{c2}\right)H_d \tag{8.48}$$

$$C_1 p V_{c1} = -I_{dc} + \frac{3}{2}\left[\alpha\left(H_q I_q{}^e + H_d I_d{}^e\right)\right] \tag{8.49}$$

$$C_2 p V_{c2} = -\left[I_{dc} - \frac{3}{2}\left[\beta\left(H_q I_q{}^e + H_d I_d{}^e\right)\right]\right] . \tag{8.50}$$

From Eqs. (8.49) and (8.50) it can be found that $\alpha = \beta$.

Hence substituting the above condition in Eqs. (8.42-8.45)

$$V_q{}^e = R_s I_q{}^e + L_s p I_q{}^e + \omega_e L_s I_d{}^e + \left(V_{dc}\right)H_q \tag{8.51}$$

$$V_d{}^e = R_s I_d{}^e + L_s p I_d{}^e - \omega_e L_s I_q{}^e + \left(V_{dc}\right)H_d \tag{8.52}$$

$$C_1 pV_{c1} = -I_{dc} + \frac{3}{2}\left[\left(H_q I_q{}^e + H_d I_d{}^e\right)\right] \tag{8.53}$$

$$C_2 pV_{c2} = -\left[I_{dc} - \frac{3}{2}\left[\left(H_q I_q{}^e + H_d I_d{}^e\right)\right]\right]. \tag{8.54}$$

8.6 Open-loop Simulation of the Rectifier

In the open loop simulation, the modulation signals are assumed such that the unity power factor condition is achieved.

8.6.1 Circuit Parameters

Input line resistance $R_s = 0.2\Omega$

Input line inductance $L_s = 10mH$

Input Supply Voltage $v_a = 80\cos(\omega t)$

$$v_b = 80\cos\left(\omega t - 120^0\right)$$

$$v_c = 80\cos\left(\omega t + 120^0\right)$$

Output dc-capacitance $C_1 = C_2 = 2200\mu F$

Load resistance $R_L = 75\Omega$

In the simulation, the modulation signals, which are calculated using the assumed voltages and currents, are compared with the two triangles to obtain the switching function. Using the equations derived in section 8.5, the converter is simulated for unity power factor condition.

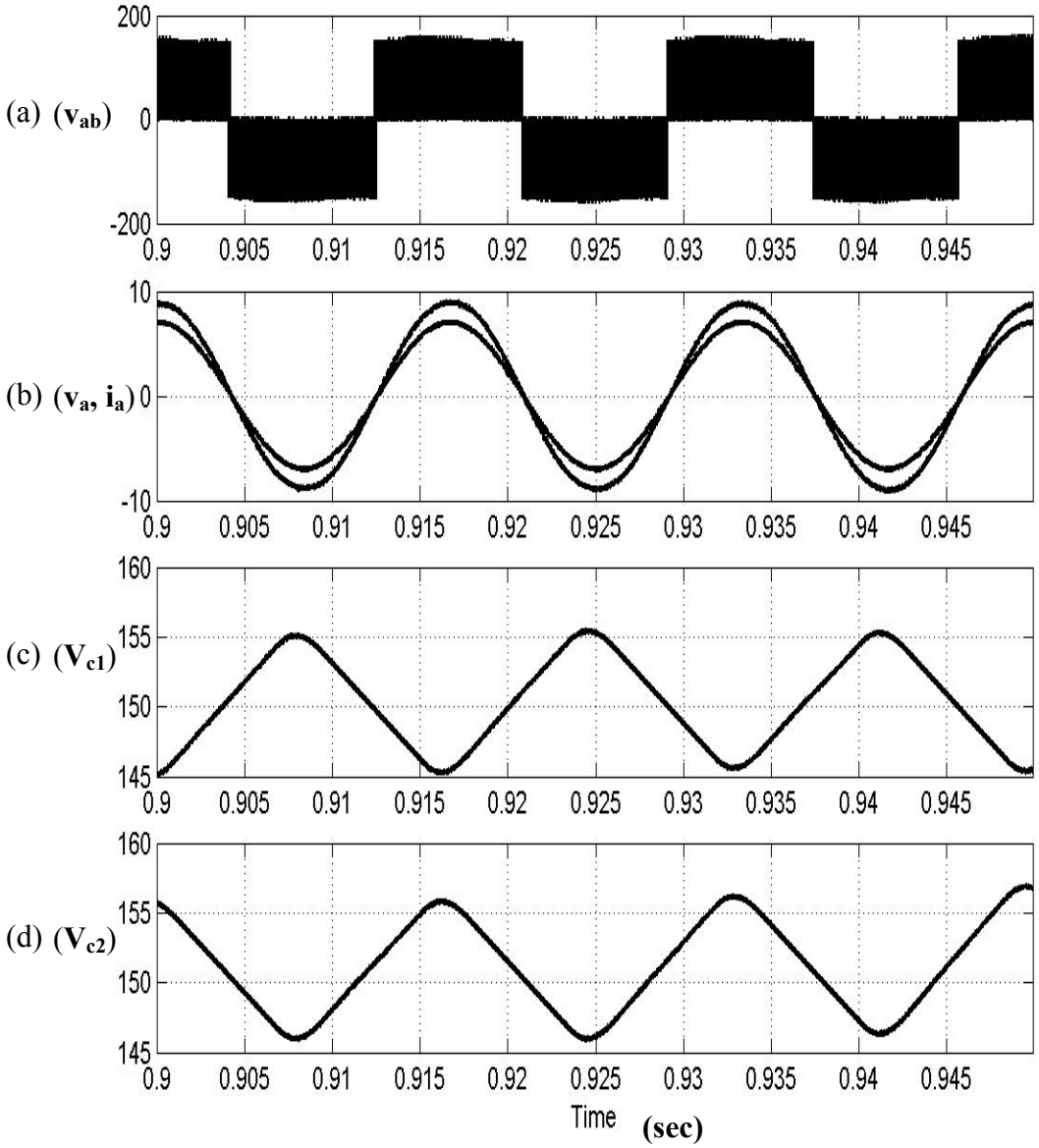

Figure 8.11: Open loop simulation of the rectifier. Operating Condition 1: $V_{dc} = 300V$. (a) Line-line voltage v_{ab} (b) Input phase voltage i_a and input phase current i_a showing the unity power factor operation (c), (d) Output Capacitor Voltages

Figure 8.11 show the open loop simulation results for unity power factor operation for an operating condition of a dc voltage of 300 V. Figure 8.11 (a) shows the line-to-line

voltage Figure 8.11 (b) illustrates the unity power factor operation in which the phase "a" voltage and phase "a" current are in phase. The capacitor voltages are illustrated in Figure 8.11 (c) and (d), which shows that the capacitors voltages are settled at 150 V each with a ripple of 5 V.

8.7 Control of Two-Leg Three phase Three-Level Rectifier

The control scheme is similar to that explained in Chapter 7 where the controllable quantities are time-varying signals and using the natural reference frame controller explained in Chapter 5 the signals are controlled. The concept of the natural variables makes the control analysis and its implementation simple.

8.7.1 Control Scheme

From section 8.4

$$v_a = i_a R_s + L_s p i_a + H_a V_{dc} + V_{20} \tag{8.55}$$

$$v_b = i_b R_s + L_s p i_b + H_b V_{dc} + V_{20} \tag{8.56}$$

$$v_c = i_c R_s + L_s p i_c + V_{20}. \tag{8.57}$$

For a balanced case, $i_c = -(i_a + i_b)$.

By substituting i_c in Eq. (8.52)

$$v_c = -(i_a + i_b)R_s - L_s p(i_a + i_b) + V_{20}.$$

To eliminate the term V_{20}, subtract Eqs. (8.55), (8.57) and Eqs. (8.56), (8.57).

$$v_{ac} = 2i_a R_s + 2L_s pi_a + i_b R_s + L_s pi_b + H_a V_{dc} \tag{8.58}$$

$$v_{bc} = 2i_b R_s + 2L_s pi_b + i_a R_s + L_s pi_a + H_b V_{dc} \ . \tag{8.59}$$

Solving for $L_s pI_a$ and $L_s pI_b$

$$L_s pi_a = \frac{-v_{bc} + 2v_{ac} + H_b V_{dc} - 2H_a V_{dc}}{3} - i_a R_s \, .$$

Rearranging the terms and simplifying

$$3\left(i_a R_s + L_s pi_a\right) = -v_{bc} + 2v_{ac} + H_b V_{dc} - 2H_a V_{dc} \, .$$

Assuming $\sigma_a = 3\left(i_a R_s + L_s pi_a\right)$,

$$\sigma_a = -v_{bc} + 2v_{ac} + H_b V_{dc} - 2H_a V_{dc} \ . \tag{8.60}$$

Similarly

$$\sigma_b = -v_{ac} + 2v_{bc} + H_a V_{dc} - 2H_b V_{dc} \ . \tag{8.61}$$

From the above Eqs. (8.60) and (8.61), solving for H_a, H_b, the modulation signals as

$$H_a = \frac{3v_{ac} - \sigma_b - 2\sigma_a}{3V_{dc}} \tag{8.62}$$

$$H_b = \frac{3v_{bc} - \sigma_a - 2\sigma_b}{3V_{dc}} \, . \tag{8.63}$$

Adding Eqs. (8.40) and (8.41) gives

$$CpV_{dc} = -2I_{dc} + 2H_a i_a + 2H_b i_b \, . \tag{8.64}$$

By substituting the expressions for H_a, H_b from Eqs. (8.62) (8.63) in Eq. (8.64)

$$CpV_{dc} = -2I_{dc} + 2\left(\frac{3v_{ac} - \sigma_b - 2\sigma_a}{3V_{dc}}\right) i_a + 2\left(\frac{3v_{bc} - \sigma_a - 2\sigma_b}{3V_{dc}}\right) i_b \, . \tag{8.65}$$

By simplifying the equation and writing in terms of the phase voltages

$$\frac{3}{2}CpV_{dc}^{\ 2} = -6I_{dc}V_{dc} + 6i_a\left(v_a - v_c\right) + 6i_b\left(v_b - v_c\right) - 2i_a\sigma_b - 4i_a\sigma_a - 2i_b\sigma_a - 4i_b\sigma_b \ . \tag{8.66}$$

For unity power factor operation

$$i_a = Kv_a \text{ and } i_b = Kv_b \tag{8.67}$$

where K is constant factor.

Substituting Eq. (8.67) in Eq. (8.66) and simplifying

$$\frac{3}{2}CpV_{dc}^{\ 2} = -6I_{dc}V_{dc} + K\left[6\left(v_a^{\ 2} + v_b^{\ 2} + v_c^{\ 2}\right) - 2\sigma_a v_{ac} - 2\sigma_b v_{bc}\right].$$

Assuming $\frac{3}{2}CpV_{dc}^{\ 2} = \delta_v$.

Solving for the value of K,

$$K = \frac{\delta_v + 6I_{dc}V_{dc}}{\Delta} \tag{8.68}$$

where $\Delta = \left\{6\left(v_a^{\ 2} + v_b^{\ 2} + v_c^{\ 2}\right) - 2\sigma_a v_{ac} - 2\sigma_b v_{bc}\right\}$.

Hence the reference frame currents can be calculated as

$$i_a^{\ *} = Kv_a$$
$$i_b^{\ *} = Kv_b.$$

The functions of the proposed control scheme are to draw the balanced and sinusoidal line currents with unity power factor, to control the dc-link voltage to be constant. To draw the balanced and sinusoidal line currents from the AC supply system, the rectifier is controlled to follow the reference line currents that are generated using the control methodology. Figure 8.12 shows the schematic of the control scheme for the

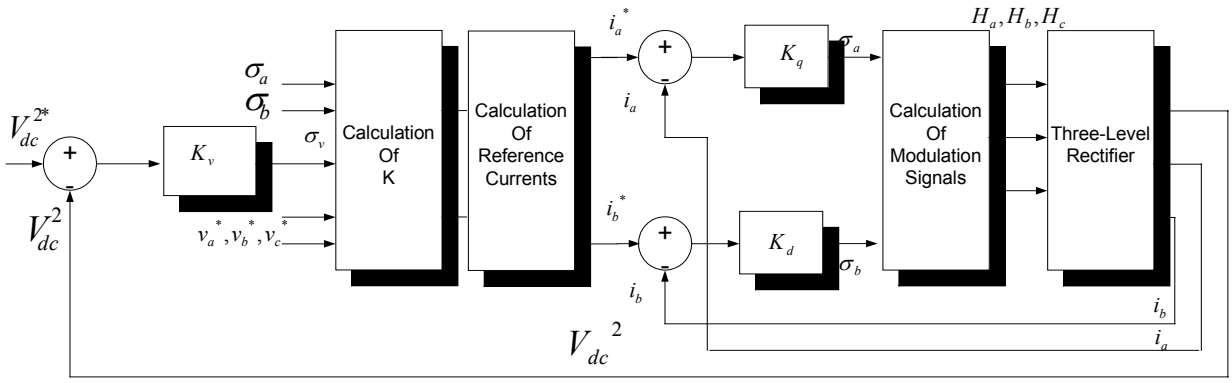

Figure 8.12: Block diagram of the control scheme.

proposed rectifier. Control scheme has a similar structure to control scheme explained in the previous chapter for a three-phase three-leg three level inverter scheme. The voltage controller acts as the outer loop and the current controllers as the inner loops. The controllers are designed such that the response time of the inner control loop is faster than that of the outer control loop. Passing the error signal through a PI controller can reduce the voltage error between the reference dc voltage and the actual dc voltage. The output of the voltage controller is used in calculating the reference currents. Natural reference frame controllers are used to track the reference currents. The output of these controllers is used in calculating the modulation signals using Eqs (8.62) and (8.63). The appropriate PWM generator is used to obtain the switching signals for the power devices.

8.7.2 Controller Structure and Design

This section presents the controller structures and the procedure to select the controller parameters. The transfer functions for the voltage controller and the current controller are derived.

8.7.3 Natural Reference Frame Controller

The transfer functions of the current controllers are derived in the similar way as explained in Chapter 5. Hence the transfer functions of the two current controllers are

$$\frac{i_a}{i_a^*} = \frac{e^{i\phi_1}(p+j\omega)[k_p(p-j\omega)+k_{ip}] + e^{-i\phi_1}(p-j\omega)[k_n(p+j\omega)+k_{in}]}{(3R_s+3L_sp)(p^2+\omega^2) + e^{i\phi_1}(p+j\omega)[k_p(p-j\omega)+k_{ip}] + e^{-i\phi_1}(p-j\omega)[k_n(p+j\omega)+k_{in}]}.$$

For simplicity, if $k_{ip} = k_{in} = k_i; k_n = k_p = k_p$, then

$$\frac{i_a}{i_a^*} = \frac{p^2 2k_p\cos\phi_1 + p2k_i\cos\phi_1 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}{3L_sp^3 + p^2\left[2k_p\cos\phi_1 + 3R_s\right] + p[2k_i\cos\phi_1 + 3\omega^2 L_s] + 3R_s\omega^2 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}.$$

Similar analysis can be done for the phase B current and the transfer function as

$$\frac{i_b}{i_b^*} = \frac{p^2 2k_p\cos\phi_1 + p2k_i\cos\phi_1 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}{3L_sp^3 + p^2\left[2k_p\cos\phi_1 + 3R_s\right] + p[2k_i\cos\phi_1 + 3\omega^2 L_s] + 3R_s\omega^2 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}.$$

In designing the parameters of the controller, by comparing the denominator of the transfer function with Butterworth Polynomial. The Butter-worth polynomial for the third order is as follows:

$$p^3 + 2p^2 w_0 + 2pw_0^2 + w_0^3 = 0. \tag{8.69}$$

Hence by comparing the denominator of the transfer function with above polynomial

$$\frac{3R_s + 2\cos\phi_1 k_p}{3L_s} = 2\omega_0 \tag{8.70}$$

$$\frac{3\omega^2 L_s + 2\cos\phi_1 k_i}{3L_s} = 2\omega_0{}^2 \tag{8.71}$$

$$\frac{3R_s\omega^2 + 2\cos\phi_1 k_p\omega^2 - 2k_i\omega\sin\phi_1}{3L_s} = {\omega_0}^3 . \tag{8.72}$$

Hence by solving above three equations for the three unknowns k_i, k_p, ω_0 and by varying the delay angle ϕ_1 the controller parameters can be calculated.

8.7.4 Voltage Controller

The voltage control structure is same as discussed in control scheme A. Hence the transfer function of the controller is as follows:

$$\frac{{V_{dc}}^2}{{V_{dc}}^{*2}} = \frac{sK_p + K_i}{Cs^2 + 2sK_p + 2K_i} . \tag{8.73}$$

The second order Butter Worth polynomial is given by

$$s^2 + \sqrt{2}s\omega_0 + {\omega_0}^2 = 0 . \tag{8.74}$$

By comparing the coefficients of same exponentials

$$K_p = \frac{C\omega_0}{\sqrt{2}} \text{ and } K_i = \frac{C{\omega_0}^2}{2} . \tag{8.75}$$

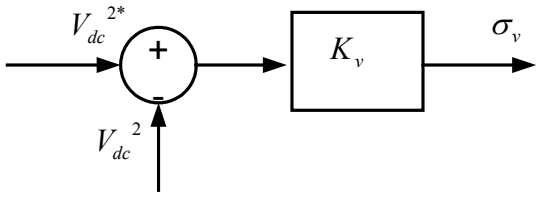

Figure 8.13: Structure of the Voltage controller.

In this case ω_0 value depends on the value of ω_0 which is obtained from the current controller. The value ω_0 of the voltage controller has to be at least 10 times lesser than that of the current controller so as to make the response time of the voltage controller slower than that of the current controller.

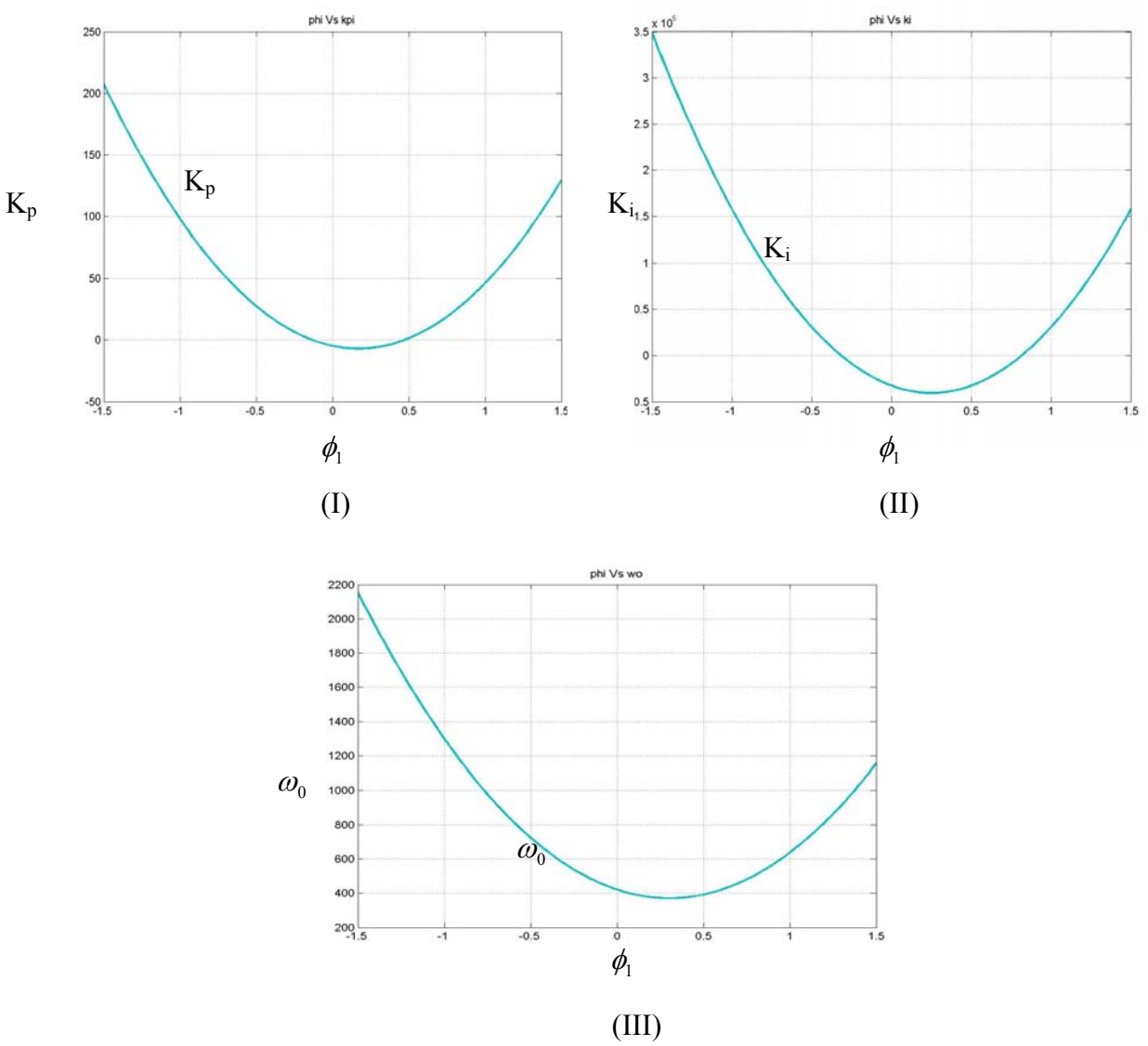

Figure 8.14: Variation of the control parameters of the current controller with the variation of the delay angle ϕ_1.(I) K_p ,(II) K_i ,(III) ω_0.

Figure 8.14 shows the variation of the control parameters of the current controller with the variation of the delay angle. The delay angle is varied from – pi/2 to + pi/2 and the expression k_p, k_i, ω_0 obtained by solving expression (8.70-8.72) are evaluated and plotted against the delay angle. After getting ω_0 from the current controller the voltage control parameters are obtained using expressions (8.75).

8.8 Simulation Results

The simulation results shown in Figures 8.15- 8.19 show the effectiveness of the control scheme. As seen from the results, it is clear that the capacitor voltage is being regulated well and the unity power factor operation both in the rectifier and the inverter mode of operation has been achieved. The circuit components of the adopted converter are $R_s = 0.2\Omega$, $L_s = 10mH$, and $C = 2200\mu F$. The peak of the input supply voltage is 80 V and source frequency is 60 Hz. The carrier frequency is 5 kHz. The reference dc-link voltage is taken as 300 V. Figure 8.15 show the modulation signals which when modulated using the carrier based PWM as explained earlier in Chapter 3 achieves the voltage regulation and the unity power factor operation in the rectifier mode of operation. Figure 8.16 I. (a) shows the line-line voltage generated at the input of the rectifier and (b) shows the unity power factor operation of the rectifier. The effectiveness of the natural reference frame controller is illustrated in Figure 8.16 (II). The figure shows the effective tracking of the reference currents. Figure 8.17 (I) and (II) gives the split dc capacitor voltages V_{c1}, V_{c2}, and shows that the capacitor voltages settled to the reference voltages of 150 V each with a ripple of 6 V. After the capacitor voltages have settled the load is

being changed such that the converter is made to operate as an inverter i.e., the power is fed from the load to the source. The change of load occurs at t = 0. 8 sec. Figure 8.17 (III) shows the change of load, in the simulation the regenerative mode is obtained by using a negative resistance of -150Ω. Figure 8.17 (IV) shows the variation of factor K which is used to calculate the reference currents and as expected the factor is a constant. Figure 8.18 (I) (a) and (b) shows the modulation signals in the inverter mode of operation. Figure 8.18 (II) (a) shows the line-line voltage; (b) illustrate the unity power factor condition where the load is supplying the power to the source with a power factor of unity. Figure 8.19 demonstrates the tracking of the reference currents. Hence the simulation results validate the proposed control scheme.

Rectifier Mode of Operation:

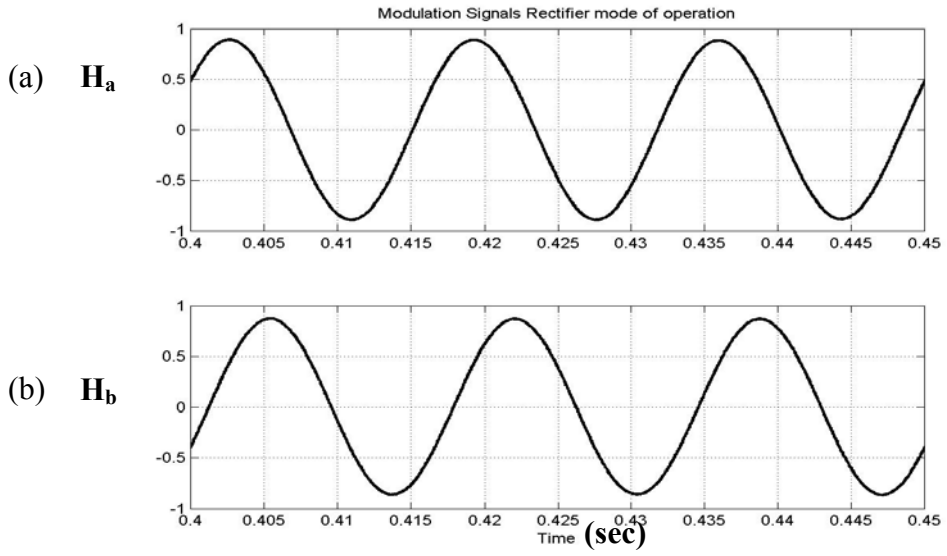

Figure 8.15: Simulation results of the control scheme: Rectifier mode of operation with a load resistance of R_L = 75Ω. (a) phase a modulation signal (H_a) (b) phase b modulation signal (H_b).

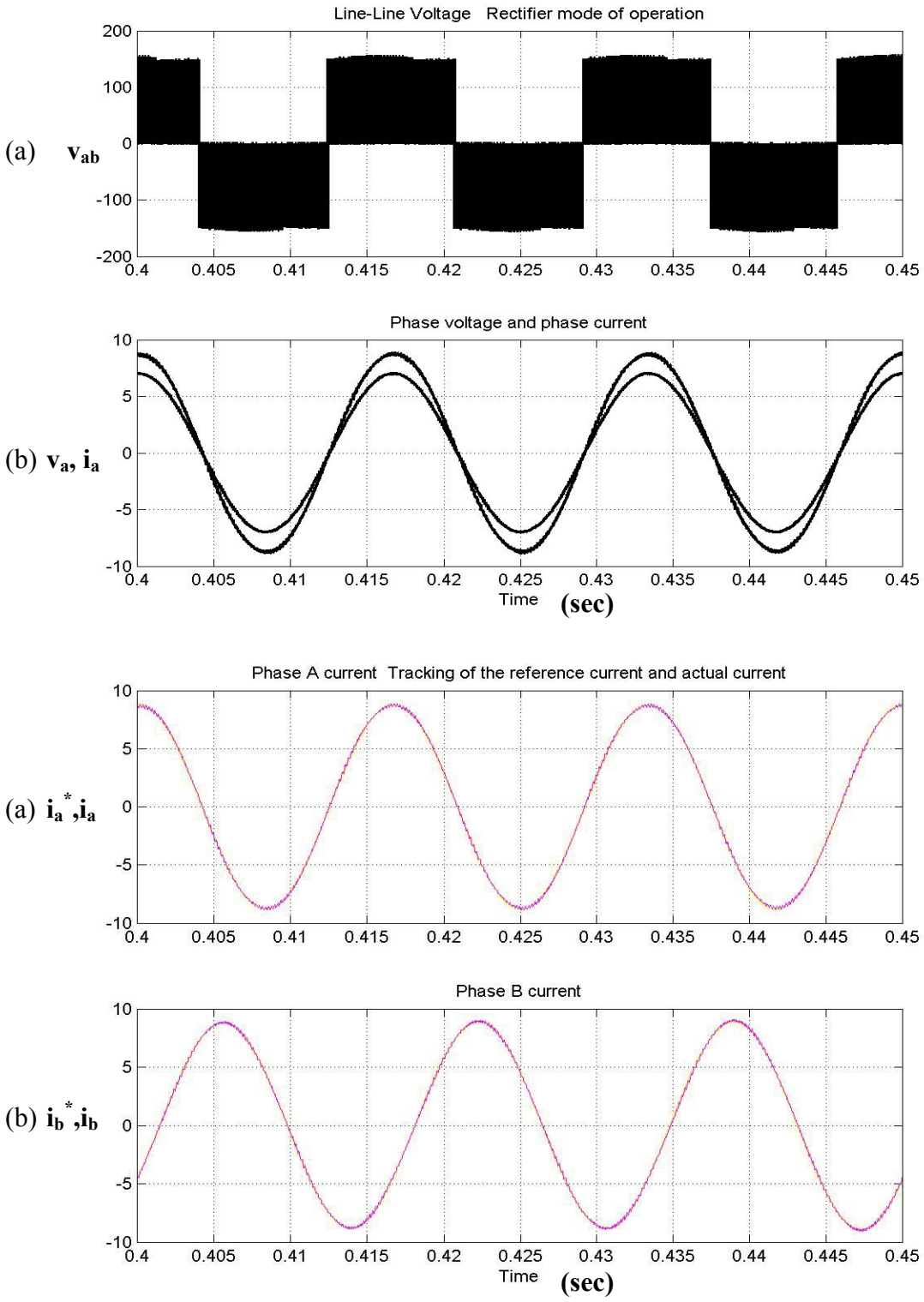

Figure 8.16: Simulation results of the control scheme. Rectifier mode of operation I. (a) Line-line voltage v_{ab} (b) Unity power factor operation, phase voltage (v_a) and phase current (i_a). II. (a),(b) tracking of the reference current and the actual current (phase-A and phase-B).

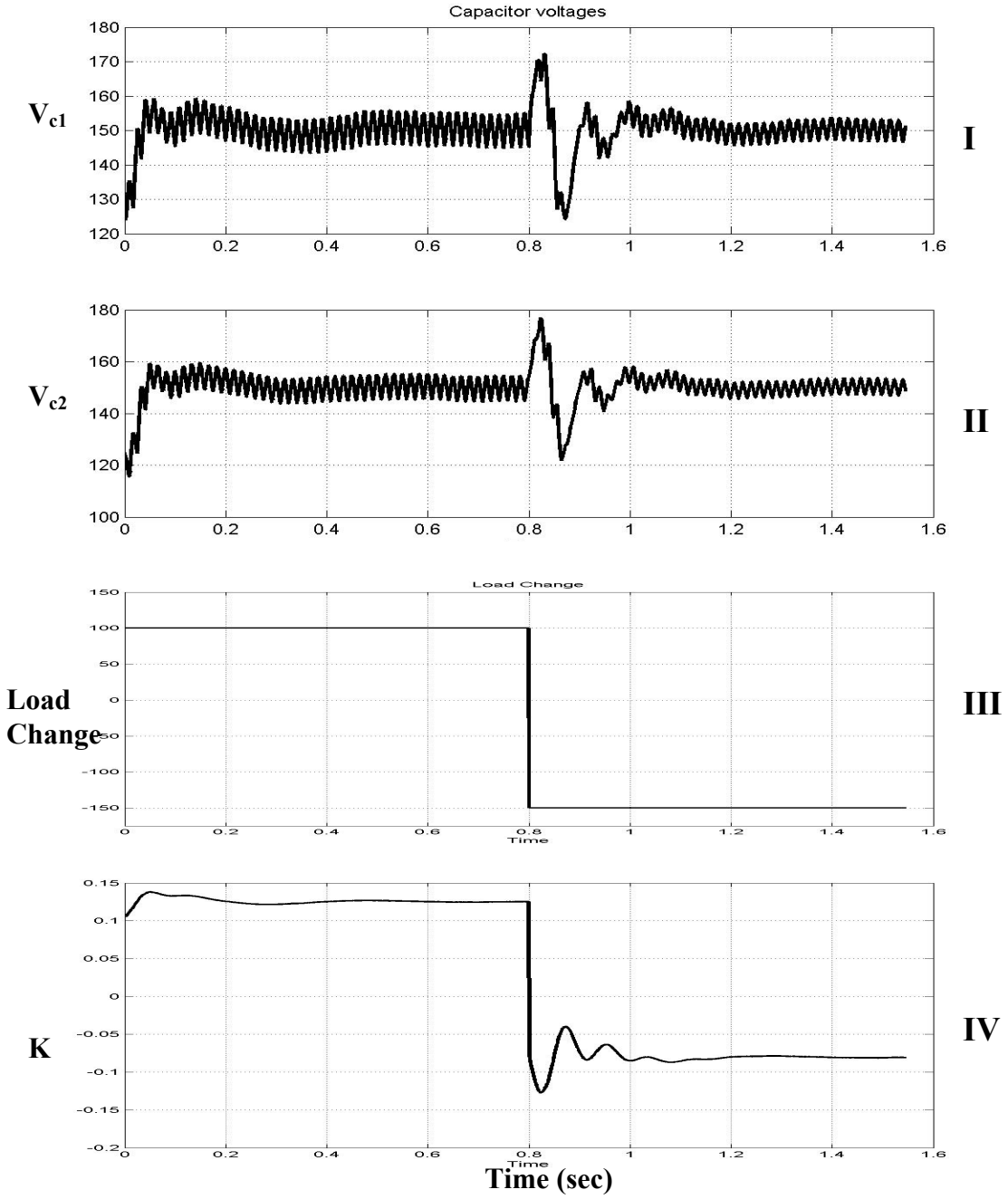

Figure 8.17: Simulation results of the control scheme. (I). Upper capacitor voltage V_{c1}, (II) Lower capacitor voltage V_{c2}, (III) Load change at t = 0.8 sec, (IV) Change of factor K.

Regenerative Mode of Operation:

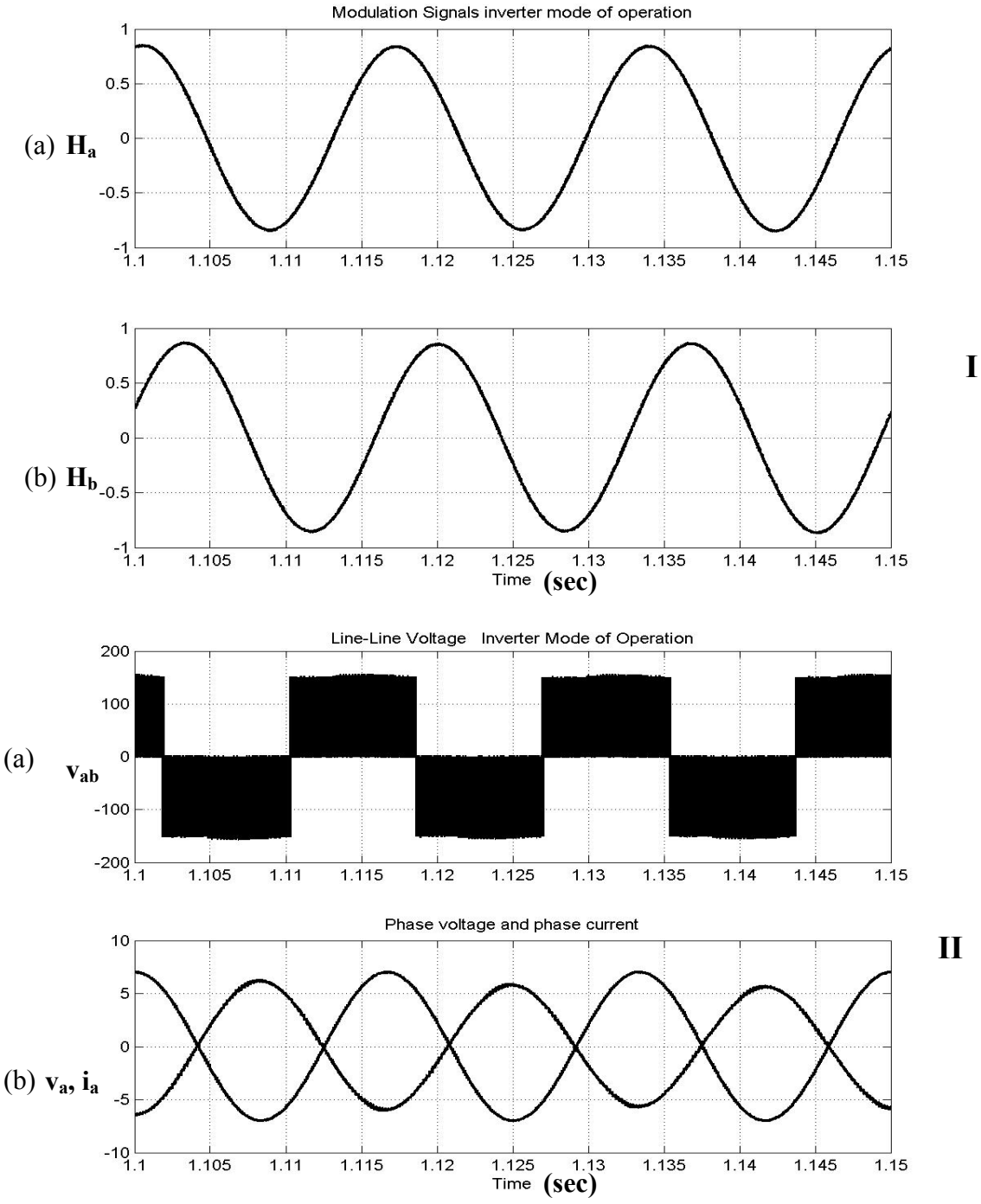

Figure 8.18: Simulation results of the control scheme. Inverter mode of operation. (I) (a), (b) Modulation signals (phase-A and phase-B), (II) (a) Line-line voltage v_{ab} (b) Phase "a" voltage and phase "a" current.

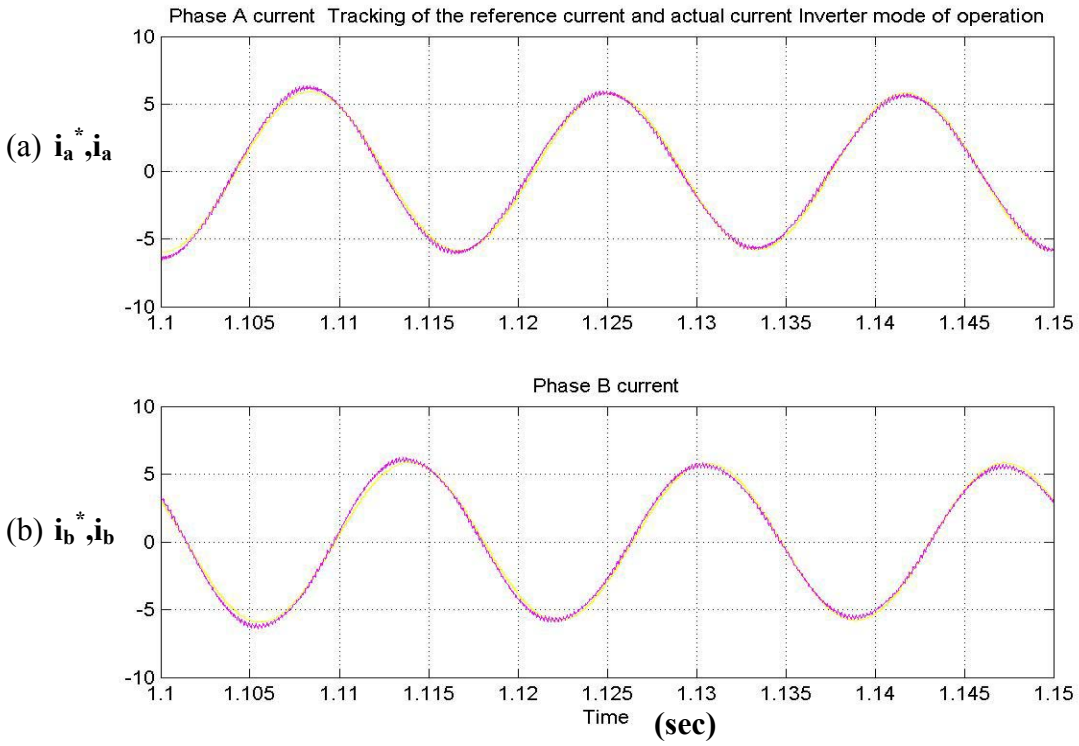

Figure 8.19: Simulation results of the control scheme. Inverter mode of operation (a), (b) tracking of the reference current and the actual current (phase "a" and phase "b").